Selectively Assembling High Value Components Based on Warpage in Order to Improve Reliability

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Abstract
Increasingly larger surface mount components are being developed in today's SMT industry. With increasing footprints, maintaining acceptable warpage levels through reflow and/or real-world use is a growing challenge. Undoubtedly, efforts are made to mitigate warpage in both PCB and components. However, there are limits to these mitigation effects and they do not resolve sample to sample variation. Here the question is posed, what if 100% of components and corresponding PCB attach areas are measured for flatness prior to assembly? Could pick-and-place machines selectively pick a "best" matching component from those available, to place on the next PCB that comes down the line?

This paper and corresponding study only lays the foundation to answer these posed questions. It is hypothesized that matching shapes at room temperature based on minimizing gap between attaching surfaces is not the optimal way to make PCB to component matching decisions. Instead, it is suggested that predicting what these shapes will be at critical points in the reflow/reliability profile is the more critical shape matching to consider. In this study, a sampling of matching footprints of PCBs and components are measured under reflow temperatures via common full-field optical metrology techniques. Critical assembly temperatures are analyzed looking to optimize which component should go with which PCB by analyzing all possible combinations through software automation. Hypothetically, this data can then correlate back to room temperature shape combinations for the best overall surface mount reliability.

Introduction
Surface warpage, or flatness, is an established source of reliability issues in surface mount devices (SMD), particularly when these surfaces are considered as they warp due to heat generated in production or real-world use [1-6]. Thermal warpage of surface mount components such are Ball Grid Arrays (BGA) and Line Grid Arrays (LGA) are subject to different industry standards from JEDEC, JEITA, and IPC, based on sample size, ball size and ball pitch [7-9]. Further SMD studies have proposed different methods of classifying and qualifying surface shape in hopes to improve the correlation in thermal warpage data and product reliability [10]. Meanwhile, Printed Circuit Boards (PCB) are less regulated for warpage in the area where an SMD may attach. Overall PCB warpage is referenced in some industry standards and technical paper, but specific warpage limits are lacking within documentation discussing warpage of SMD landing areas [11-12]. Finally, further studies have considered warpage of both SMD and PCB landing area together [13-14].

In this study the approach of considering shape of both sides of a surface mount interface is used as the basis for the study. To fully understand warpage gaps that create defects, both sides of the attaching interface are required. The trend for larger BGA packages in high-speed network applications is furthering the need for managing warpage on both SMD and PCB side of the assembly [15]. Larger package footprints allow for more lateral space in which shape change can occur due to either starting sample shape or thermal warpage.

While measuring samples for thermal warpage is a common practice, this study is proposing a much different approach to improve product reliability. This study presents a concept of measuring warpage on 100% of high value SMD devices and 100% of the PCB landing areas where they would attach in assembly, then deciding which sample to place on which PCB. This study is very much a first step and does not provide a final approach or hardware configuration to accomplish such a quality control approach. Matching initial surface shape alone to minimize initial gaps between BGA and PCB landing sites may also be a value add and simpler approach. However, gaps at high temperature points in the reflow profile are more problematic for creation of surface mount defects [16]. Therefore, this study focuses on the ability to predict what shape will be during reflow, based on a sampling of thermal warpage data and 100% measurement of room temperature shape. Thermal warpage testing is often considered destructive, thus cannot be used for 100% inspection in production.

Experimental Methodology
Warpage Metrology Approach
Shadow Moiré and Digital Fringe Projection (DFP) warpage measurement techniques are discussed in this study. Both are referenced in industry standards related to warpage, though DFP is excluded from JEITA standards on package warpage [7-10]. Shadow Moiré is exclusively used for the data of this study, focused on accurate thermal warpage behavior of SMDs and PCB local areas. This technique is best used for continuous surfaces and provides a highly accurate approach whose accuracy

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does not scale with larger areas of measurement [17]. Though Shadow Moiré may be viable for the production room temperature measurements, here DFP is hypothesized to be the preferred approach for 100% room temperature measurements, being the more portable of the two techniques.

Shadow Moiré measures surface shape by shining a line light through a Ronchi rule grating, a piece of glass with alternating clear and opaque lines, having a common pitch from 50-500 microns. This creates a contour map via an interference pattern generated between the lines and the shadow cast by the same lines. A phase stepping technique is also applied for increased resolution. Figure 1 shows the Shadow Moiré concept, and Figure 2 shows a created contour pattern.

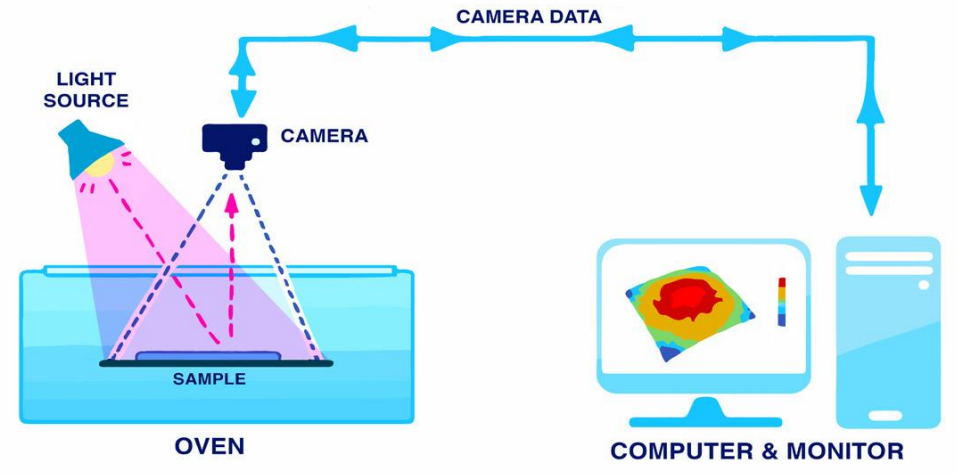

Figure 1. Shadow Moiré Visual Concept

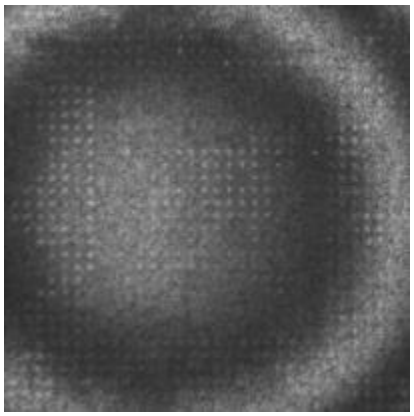

Figure 2. Shadow Moiré Pattern

DFP also measures surface shape and uses a phase stepping approach to improve resolution. Calibration is achieved by measuring an optical flat at different heights. Here a pattern is projected instead of an interference pattern created. The calibration flat and measured sample are compared to show surface shape. Fringe density can be varied as well as shifted, limited by the projector resolution only. Varying fringe pitch helps in measuring sudden sample height changes. Figure 3 shows the DFP technique and Figure 4 shows a surface with fringes projected on dome like contours on an overall flat surface.

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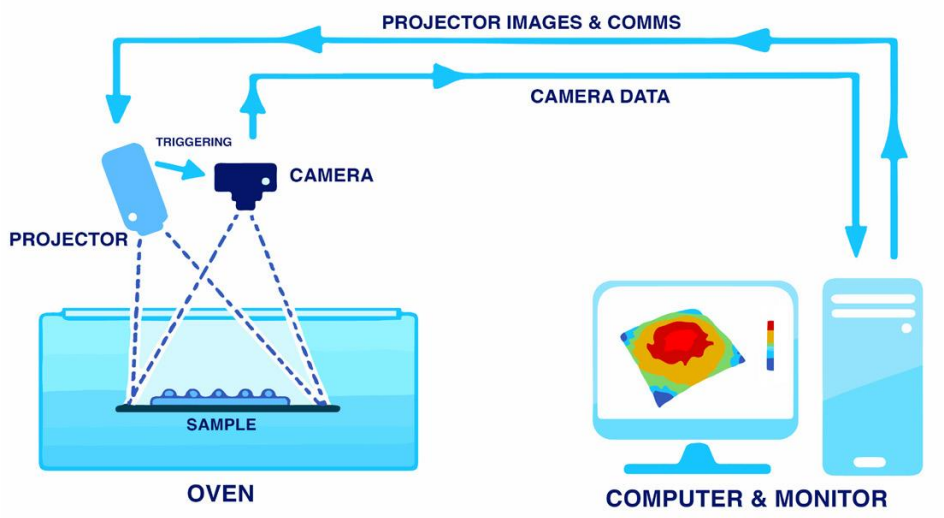

Figure 3. Digital Fringe Projection Visual Concept

Figure 4. Digital Fringe Projection Pattern

Test Samples

For the purposes of intellectual property protection sample descriptions and details are left generic for the purposes of this study. Here only a conceptual approach is presented and not details on specific samples and their warpage behavior. The purpose of testing these samples is to show how thermal warpage can be correlated to initial room temperature shape for the purposes of predicting surface mount defects. This also addresses the specific functions, such as matrix subtraction and averaging, to implement such as approach.

Multiple samples of two package types are measured for warpage across reflow temperatures. Additionally, a couple of PCBs are measured for warpage. Local areas sized to match the footprint of the package sizes will be used for comparison of warpage between package and PCB area. Details of the test samples and quantities are shown in Table 1 below.

Table 1. Test Samples

Sample Type	Sample Dimensions	Quantity Tested
Larger BGAs	75 x 75 x 2 mm	4
Smaller BGAs	32.5 x 32.5 x 2 mm	6
PCBs	237 x 255 x 1.5 mm	2 (with 2-3 local areas used)

Test Setup

Samples were prebaked 24 hours at 125°C, to reduce possible effects on warpage from moisture in the samples [18]. Oven setting were optimized around sample temperature uniformity, per standard operating procedures. All samples were subject to the same thermal profile shown in Figure 5 below.

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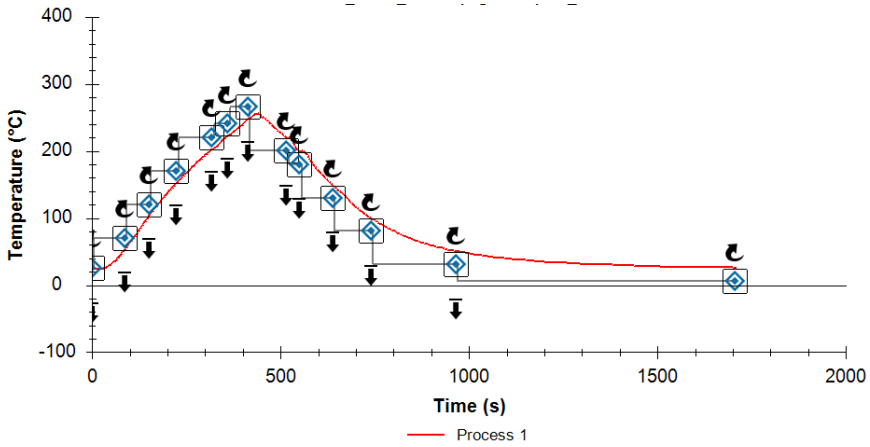

Figure 5. Thermal Profile Output

Smaller package samples were supported on Robax glass with controlling thermocouple attached to the top surface of a dummy sample for testing. The larger package samples were supported by the metal rails along the horizontal edges with a controlling thermocouple on the bottom surface. There were test setup samples with both top and bottom surface thermocouples run with the thermal profile used in all subsequent tests to optimize the oven time and temperature settings to ensure a top/bottom uniformity of +/-5°C or less. PCBs were tested on metal rails held from the edges with thermocouple attachment to the bottom surface. All other test setup variables were kept the same between sample measurements. Example setup of the package and PCB samples are shown in Figure 6 and Figure 7 below.

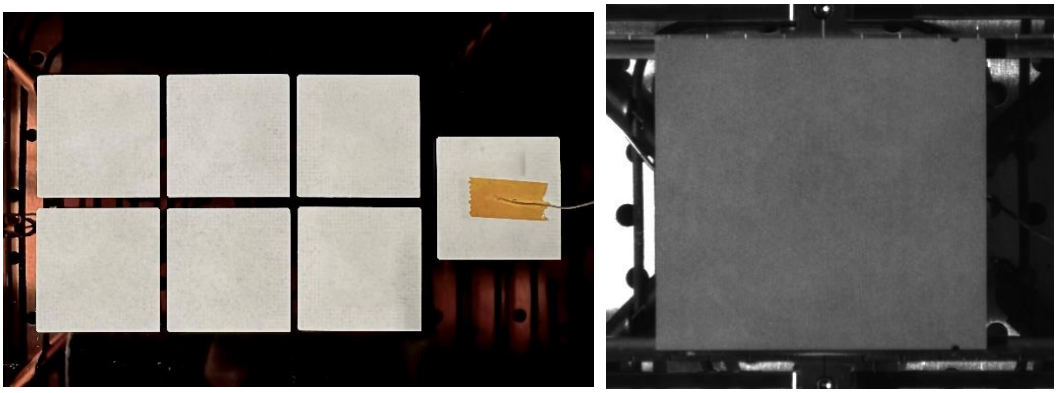

Figure 6. Package Samples (Smaller BGAs: left, Larger BGAs: right) Test Setup in Oven

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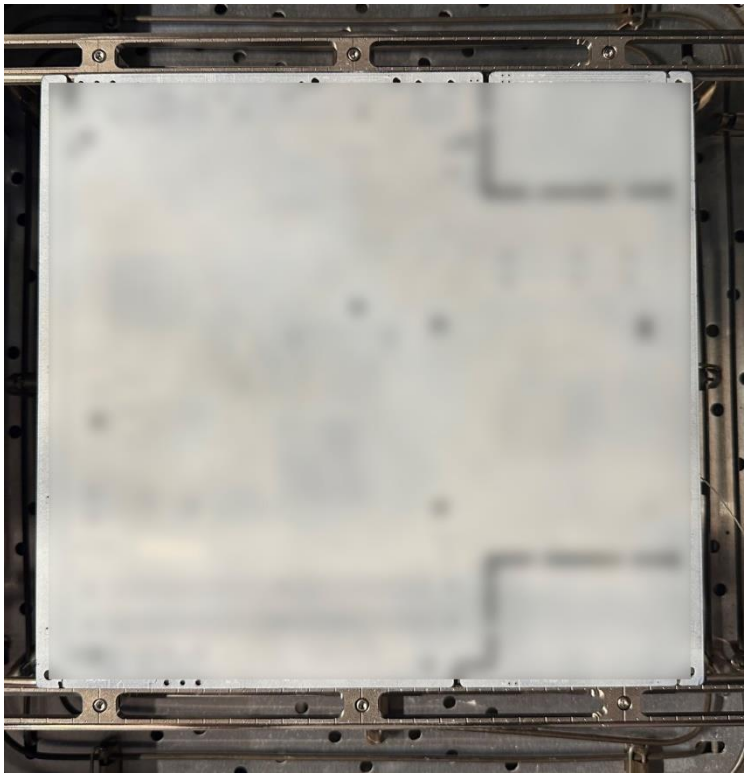

Figure 7. PCB Sample Test Setup in Oven (Blurred to Protect Manufacturer)

Shape Matching

Here only 2 PCBs are tested. Different local areas from the PCB are digitally extracted to match the specific size of the BGA land area. For the smaller BGA, 3 local areas are chosen around the PCB, thus 2 PCBs x 3 local areas are compared across temperature to the 6 smaller BGA samples. Similarly, 2 local areas are chosen with physical size matching the larger BGA, thus 4 regions of comparison are created across temperature. Note that the BGAs and PCBs are not specifically units that are assembled together in a real-world production scenario.

Offset methods and gauge choices to quantify 3D shape are another critical decision. In this study, Closest Point Touching is exclusively used as the offset method. This addresses how top and bottom surfaces are combined together for comparison. With all offset methods, sample Pin 1 location and Measured Surface, inner or outer, are tracked in sample Metadata for use in software comparisons. For gauges, maximum gap will be the data focus. However, other gauges such as average gap and compatibility could be useful gauges to consider. These gauges are defined as follows:

- Closest Point Touching: Offset Method - The Top and Bottom surfaces are brought together with their LSF (Least Squares Fit) planes parallel until the first point touches.
- Maximum Gap: The maximum distance between the top and bottom surface out-of-plane.
- Average Gap: The average distance between the top and bottom surface out-of-plane.
- Compatibility: The RMS (Root Mean Square) deviation between the top and bottom surface out-of-plane.

Room Temperature Interface Analysis

The most basic iteration of using shape matching to decide mating surfaces is purely to consider both shapes at room temperature only. In Figure 8, artificially created surfaces are used to demonstrate the concept.

In Figure 8, flipping Top Surface 1 onto Bottom Surface 1 as they would be assembled creates a surface with no gap, a fully flat plane. The same is true for Example 2 and 3. However, assembling Top Surface 3 onto Bottom Surface 1 would create a surface with significant shape between the mating surfaces as show in Figure 9.

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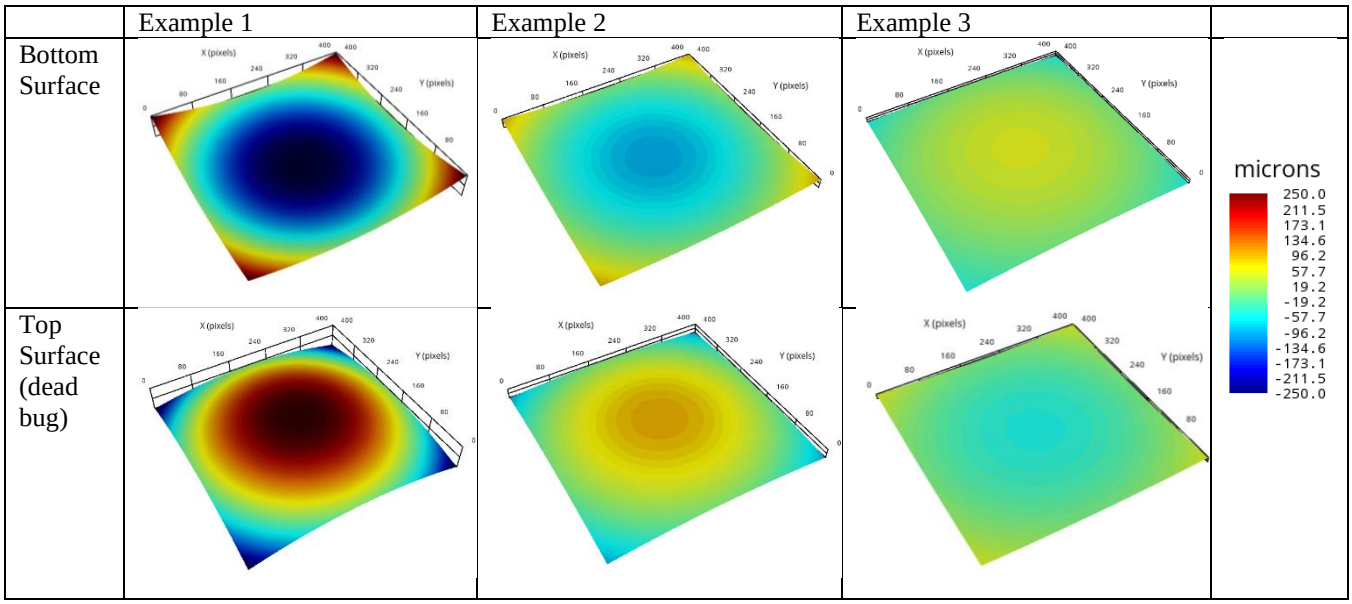

Figure 8. Surface matching example

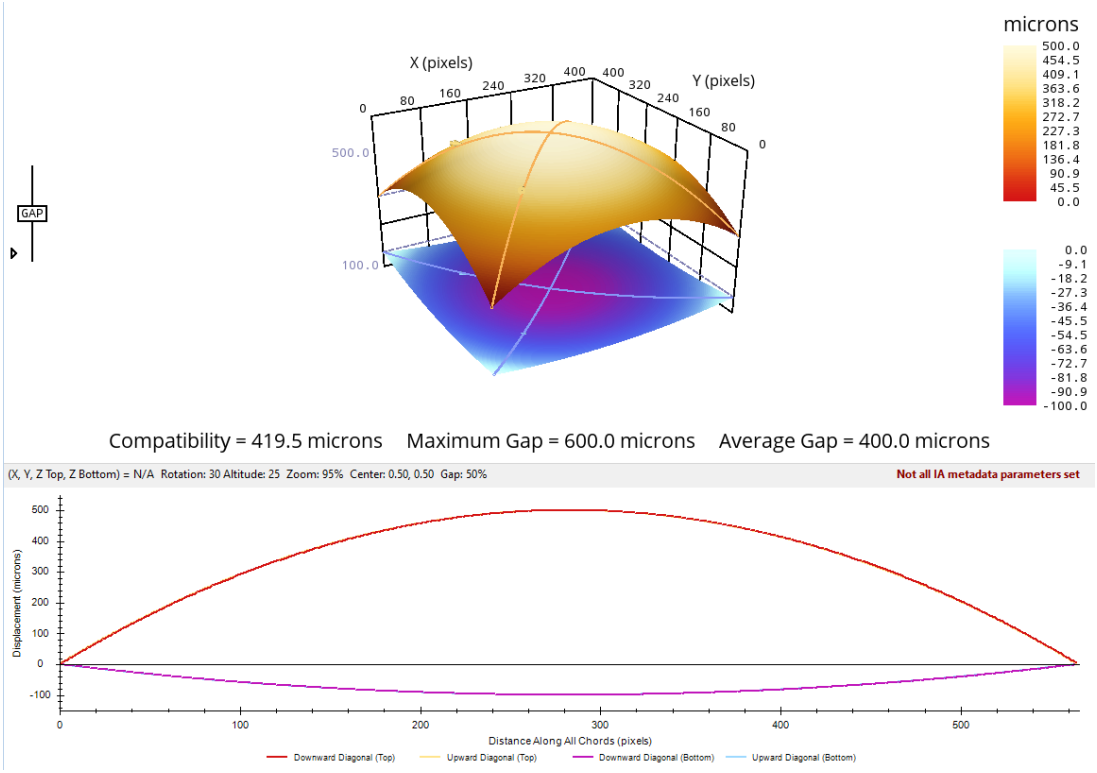

Figure 9. Interface Analysis of Poorly Matched Mating Surfaces

Figure 9 shows the potential importance of selectivity in which samples to mate. In a real-world scenario, the differences between samples are unlikely to be this extreme, but studies have shown that sample variation even at room temperature can affect product yield [19].

Prediction of Relative Shape Change in Thermal Warpage

While matching surfaces based on room temperature shape is a possible approach to improve yield, here the argument is made that a prediction of what surface shapes will be at a critical point during reflow is the more valuable data point. Around solder liquidus is of particular interest for good solder joints. It is hypothesized here that a collection of thermal warpage data can be used to predict the relative shape change of a surface over temperature. To create this data set, relative shape change from

room temperature to solder liquidus is rendered. These surface matrices are then averaged together to predict the relative shape change of the sample using only room temperature data. Examples of this process are shown in actual measurement results.

Results

Data was taken through a full reflow profile as shown in Figure 5. However, only room temperature shape and shape at 220°C on the cooling side of the profile is analyzed in this study. Warpage result gauges are presented in microns throughout.

Room Temperature Interface Analysis

Table 2 shows the maximum gap in microns at room temperature of the 6 smaller BGAs interfaced with PCB1 and 2 at all 3 ROI (regions of interest), considering every possible combination. Figure 10 shows one example interface graphically.

Table 2. Room Temperature Maximum Gap of all Interface Combinations, Smaller BGA

	BGA 1	BGA 2	BGA 3	BGA 4	BGA 5	BGA 6
PCB1-ROI1	592.6	533	522.4	504.5	533.6	596
PCB1-ROI2	621.3	562.6	544.4	533.6	562.3	592.1
PCB1-ROI3	626.9	567.4	575	538.8	567.7	648.1
PCB2-ROI1	617.7	557.6	540.2	530.2	558.7	592.4
PCB2-ROI2	585.7	527.6	509.3	507.2	526.7	554.7
PCB2-ROI3	614.6	555.9	534.9	527	553.4	588.5

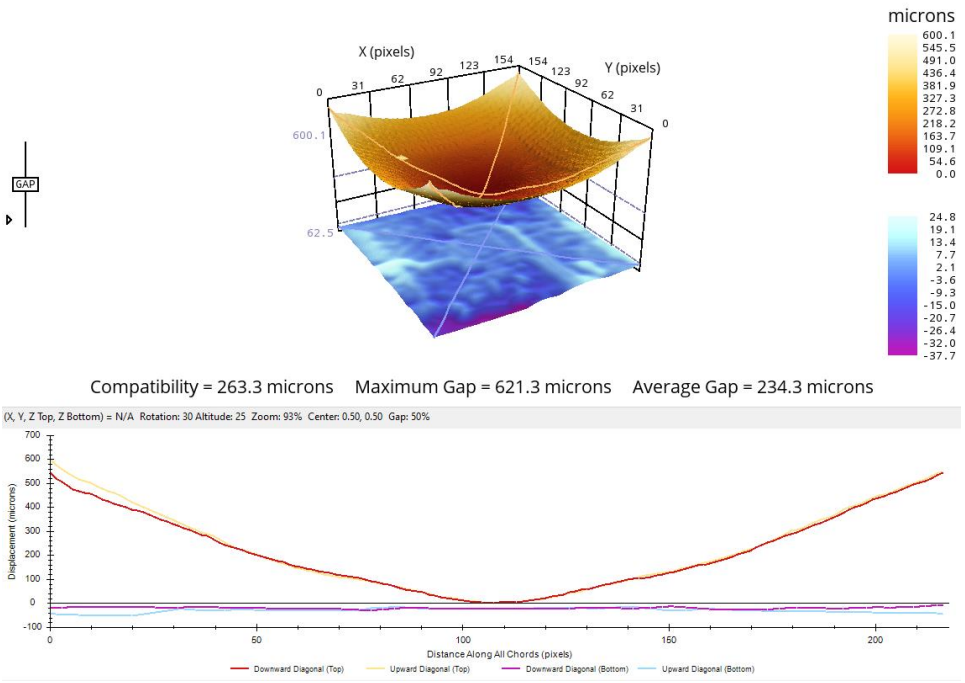

Figure 10. Room Temperature Interface Analysis between Smaller BGA 1 and PCB 1 – ROI 2

Table 3 shows the maximum gap in microns at room temperature of the 4 larger BGAs interfaced with PCB1 and 2 at 2 ROI, considering every possible combination. Figure 11 shows one example interface graphically.

Table 3. Room Temperature Maximum Gap of all Interface Combinations, Larger BGA

	BGA 1	BGA 2	BGA 3	BGA 4
PCB1-ROI1	117.8	123.5	131.1	132.8
PCB1-ROI2	170.3	172.3	216.9	196.5
PCB2-ROI1	170.8	166.3	195.3	166.5
PCB2-ROI2	356.1	369.3	371.2	404.5

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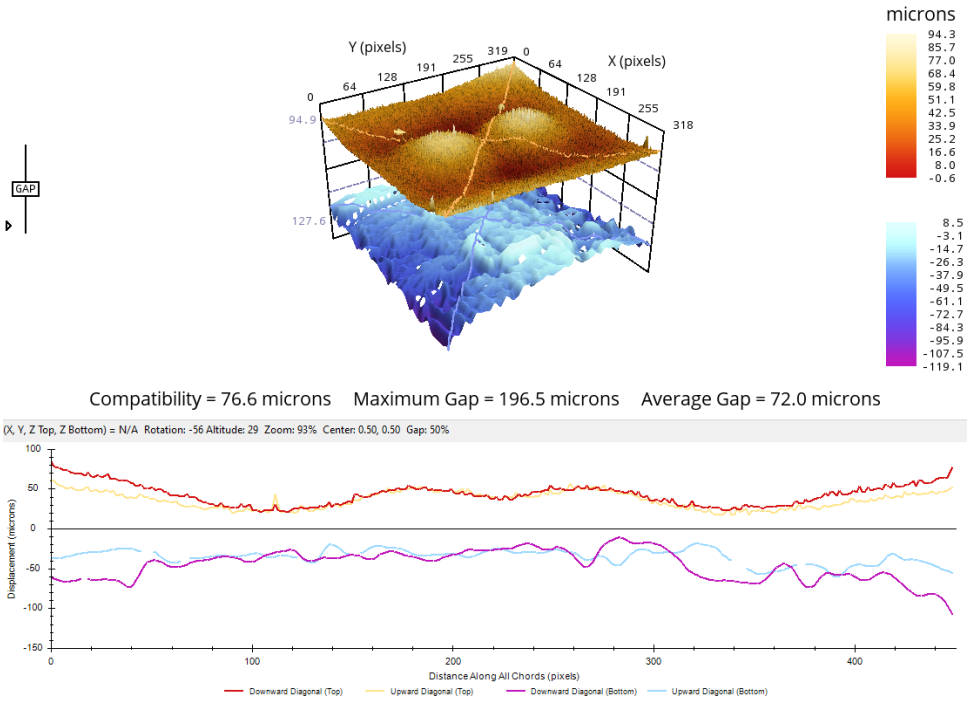

Figure 11. Room Temperature Interface Analysis between Larger BGA 4 and PCB 1 – ROI 2

Interface Analysis at Actual Solder Liquidus

Since we have thermal data for all samples, here we analyze interface gaps at a solder liquidus of 220°C on the cooling side of the profile. Later this shape will be predicted using an average of relative shape change from room temperature to 220°C. Table 4 shows the maximum gap in microns at 220°C of the 6 smaller BGAs interfaced with PCB1 and 2 at all 3 ROI, considering every possible combination. Figure 12 shows one example interface graphically.

Table 4. Solder Liquidus (220°C) Maximum Gap of all Interface Combinations, Smaller BGA

	BGA 1	**BGA 2**	**BGA 3**	**BGA 4**	**BGA 5**	**BGA 6**
PCB1-ROI1	376	456.9	430.8	482.3	422.7	447.7
PCB1-ROI2	362.1	439.5	417.9	454.9	404.9	420.9
PCB1-ROI3	335.9	408.8	381.4	447.1	362.1	383.2
PCB2-ROI1	353.6	438.1	419.3	455.5	405.4	426.4
PCB2-ROI2	374.2	452.4	411.3	462.3	403.4	411.8
PCB2-ROI3	364.8	442.6	441.1	446.5	404	436.7

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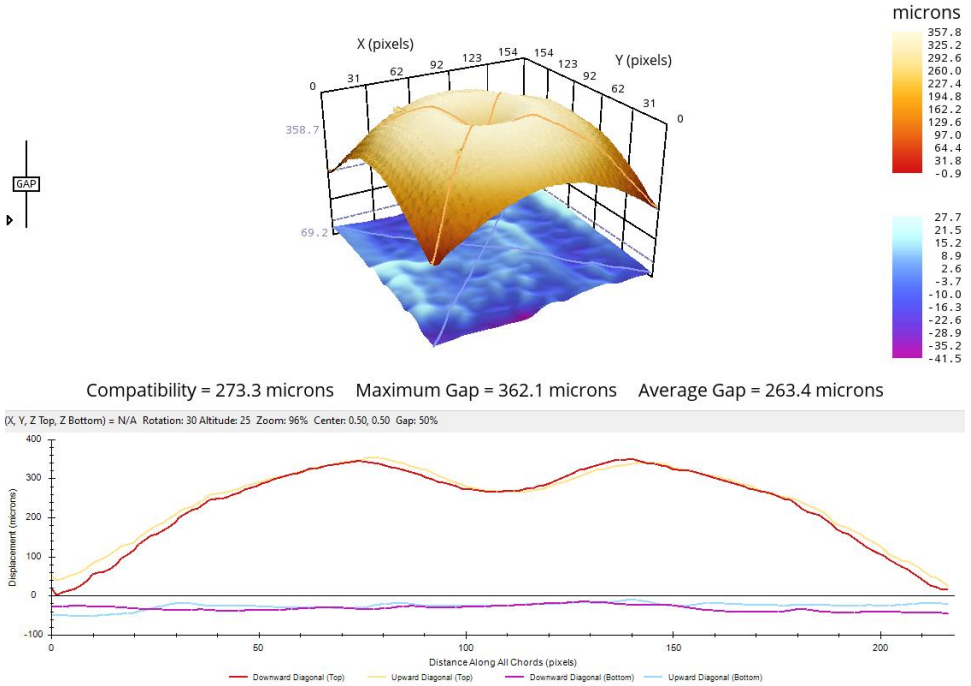

Figure 12. Solder Liquidus (220°C) Interface Analysis between Smaller BGA 1 and PCB 1 – ROI 2

Table 5 shows the maximum gap in microns at solder liquidus of 220°C of the 4 larger BGAs interfaced with PCB1 and 2 at 2 ROI, considering every possible combination. Figure 13 shows one example interface graphically.

Table 5. Solder Liquidus (220°C) Maximum Gap of all Interface Combinations, Larger BGA

	BGA 1	BGA 2	BGA 3	BGA 4
PCB1-ROI1	151.2	145	158.7	149.2
PCB1-ROI2	246.5	249.5	250.7	280.7
PCB2-ROI1	208.4	208.6	239.7	210.8
PCB2-ROI2	237.6	229.9	253.8	260.1

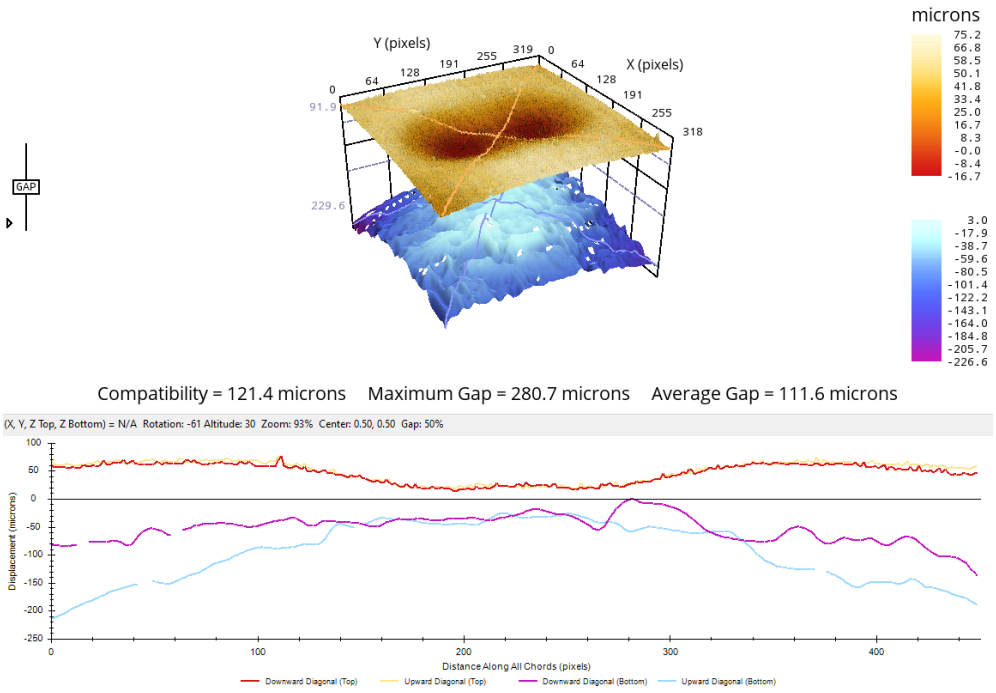

Figure 13. Solder Liquidus (220°C) Interface Analysis between Larger BGA 4 and PCB 1 – ROI 2

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Relative Shape Change Room Temperature to Solder Liquidus

For each measured surface, the relative shape change between room temperature and 220°C can be found by subtracting the room temperature surface from the 220°C surface as in Figure 14.

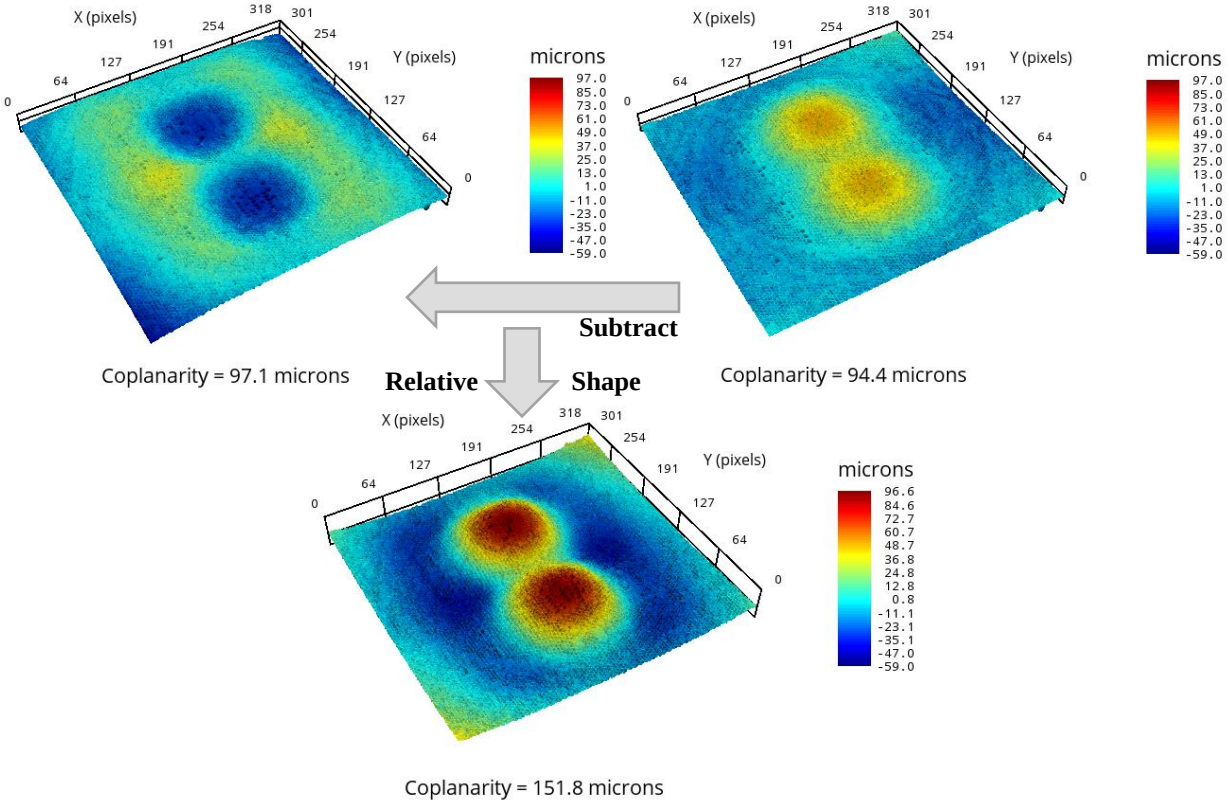
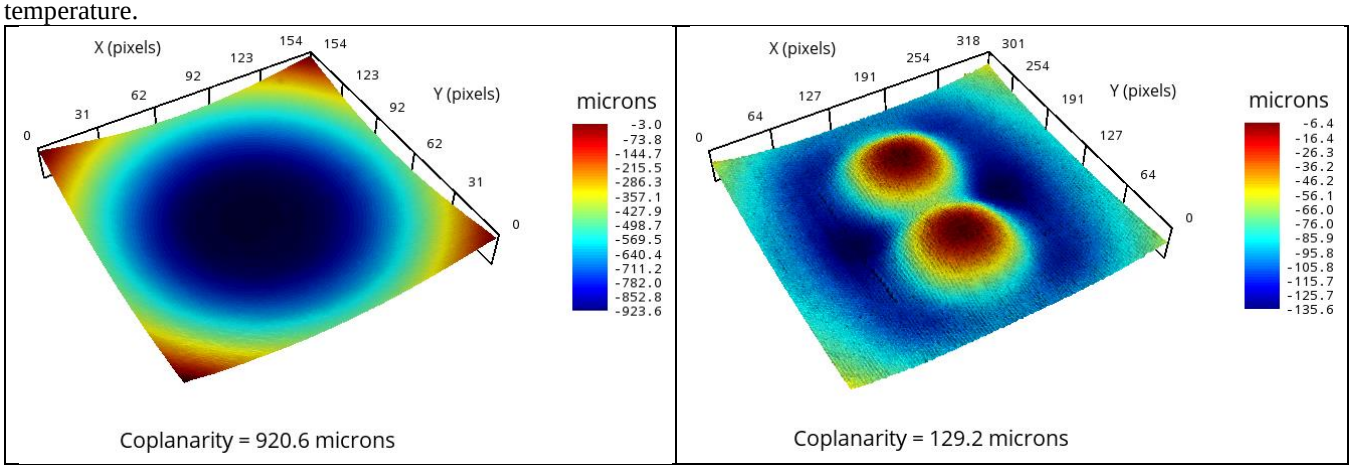


Figure 14. Relative Shape Change in BGA 4 from Room Temperature to 220°C

This process is repeated for all surface data. Then relative surfaces for each ROI are averaged together. Figure 15 shows the 4 average relative warpage change surfaces for the PCB and BGA in larger and smaller sizes between 220°C and room temperature.



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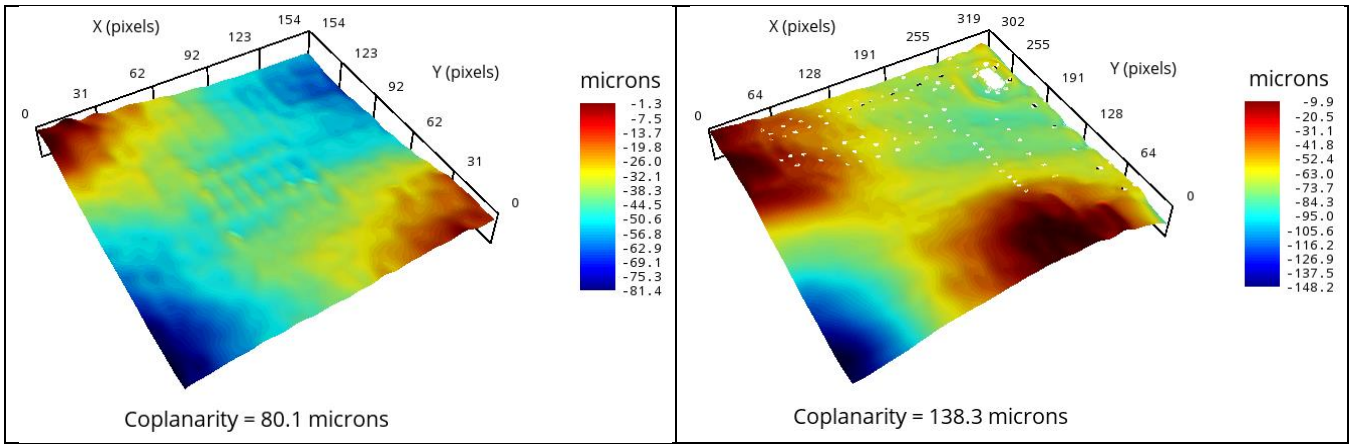

Figure 15. Average Relative Shape Change from Room Temperature to 220°C; Smaller BGA (top left), Larger BGA (top right), Smaller PCB all ROI (bottom left), Larger PCB all ROI (bottom right)

Prediction of Shape at Solder Liquidus Based on Average Shape Change

The final step is to use these averaged surfaces, applying the shape change to the room temperature surface to try and predict what the shape will be at the critical solder liquidus point in the reflow profile. The example from Figure 14 can be used again below in Figure 16. The average relative shape change is inverted and then subtracted from room temperature data to predict the solder liquidus shape.

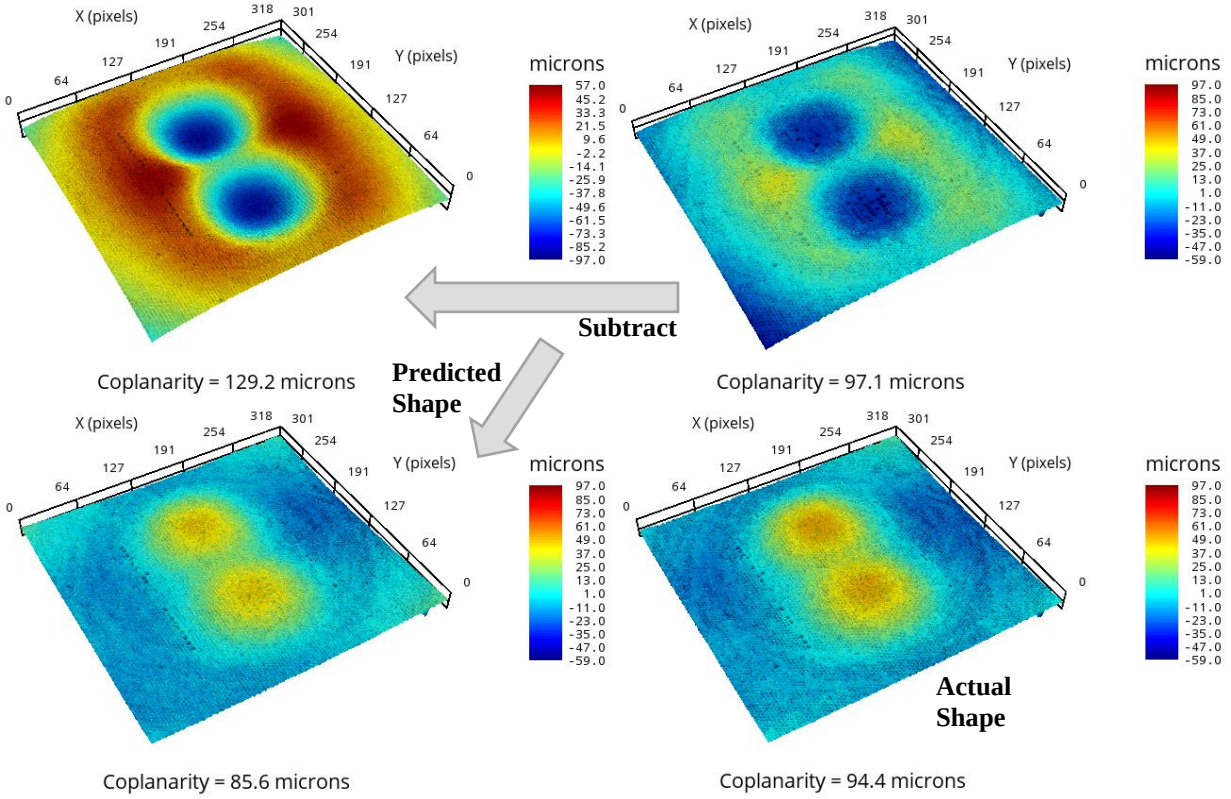

Figure 16. Predicted Larger BGA Shape at 220°C based on Room Temperature Shape and Average Relative Shape Change

This same process can be repeated for all surface to recreate max gap numbers using the relative shape change prediction and actual room temperature shape of both PCB and BGA surfaces. The hope is to find similar numbers found in Tables 4 and 5. Given the highly different shapes change of the multiple PCB regions, only ROI 1 from the PCB data is used in this process.

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The overall concept of this predictive method is that shape change over temperature is somewhat repeatable for samples of equal design and production conditions. Tables 6 and 7 show the results from the transformed room temperature data.

Table 6. Predicted Maximum Gap at Solder Liquidus of Interface Combinations, Smaller BGA

	BGA 1	BGA 2	BGA 3	BGA 4	BGA 5	BGA 6
PCB1-ROI1	455.4	597	486	534	490.9	424.2
PCB2-ROI1	454.5	593.8	461.3	529.9	486.7	395.2

Table 7. Predicted Maximum Gap at Solder Liquidus of Interface Combinations, Larger BGA

	BGA 1	BGA 2	BGA 3	BGA 4
PCB1-ROI1	154.8	167.4	204.4	190.2
PCB2-ROI1	179.1	197.7	214.5	200.5

Discussion

Shape Prediction Accuracy

Further data analysis starts with qualifying the accuracy of the predictive approach in using average relative change over temperature to predict sample shape at temperature. Tables 8 and 9 show the percentage error of actual maximum gap between interfaces at 220°C and the predicted gap.

Table 8. Prediction Error of Maximum Gap at Solder Liquidus of Interface Combinations, Smaller BGA

	BGA 1	BGA 2	BGA 3	BGA 4	BGA 5	BGA 6
PCB1-ROI1	28.5%	35.5%	10.0%	16.3%	20.1%	-7.3%
PCB2-ROI1	21.1%	30.7%	12.8%	10.7%	16.1%	-5.2%

Table 9. Prediction Error of Maximum Gap at Solder Liquidus of Interface Combinations, Larger BGA

	BGA 1	BGA 2	BGA 3	BGA 4
PCB1-ROI1	16.4%	5.5%	11.7%	5.1%
PCB2-ROI1	-2.3%	-13.4%	-22.4%	-21.6%

The error in the prediction is significant. However, this could be attributed to the age and unknown history of the samples used. The PCBs and small BGA were both older products with unknown thermal history. Realistic samples to the application may see different results under this presented model. Notably, the larger BGA was the more realistic and more modern package used in the study, and it showed more consistent change under reflow temperatures. While error was significant in Table 9, predictions are consistently high for PCB1 and low for PCB2, suggesting variation in the PCB could be the larger inconsistency. Larger data sets may also aid in establishing a baseline relative thermal warpage change.

Practical Production Implementation

The approach proposed in this study assumes a percentage of destructive thermal warpage testing on samples in question. This is an industry practice used by many companies, with referenced standards [7-9, 11]. However, it also assumes 100% flatness inspection of both bare PCB surface mount attach areas, as well as flatness measurement of designated high value components. Flatness inspection of these items it not a standard industry practice.

Physical space and methodology to take these measurements must be considered. PCBs would need to be measured before solder paste application. Measuring components within tape and reel is likely unrealistic. However, many high value components will be presented to pick and place machinery in JEDEC trays, making automated flatness inspection during assembly more viable. Components in JEDEC trays would also typically be sitting live bug, such that the topside is visible for measurement instead of the attach side. Industry standards for thermal warpage instruct measurement of the attach side, but they also include removal of solder balls when present, which is not practical for production, given the destructive nature [7-8]. Therefore, correlation of the shape on top of the sample may be needed, unless further complexity is added to inspect the attach side of the component. Even in this case, BGA components have the challenge of measuring substrate surfaces between the solder balls, which presents some metrology challenges for more densely populated components. However, with the availability of optical metrology techniques measuring sample shapes can be done at high speeds relative to typical reflow production processes and are not expected to increase production times.

Communication with pick and place machinery would be required to implement such a solution. However, the level of communication required would be highly simple, only needing to indicate which samples should be picked up next. Additionally, possible physical integration between pick and place tools and JEDEC loading mechanisms may be required. Measuring samples as they are loaded into the pick and place tool would be a likely place to capture component shape, possibly

taking multiple measurements per tray in order to improve measurement resolution, versus requiring motion systems for the metrology optics or multiple optical hardware setups.

The quantity of available data upon which to make decisions would be dependent upon the timing of the assembly process. The discussed examples assume that a handful of data is available at the same time in order to place combinations of samples together. The criteria for making this decision could be numerous, including many different types of gauges, including the referenced average gap and compatibility gauges. This could potentially also include a level of criteria that would fail inspection and be removed from the assembly process. A failure level is not required for the approach.

The portability of the DFP technique may be a better fit for a production scenario. Studies have shown that DFP and shadow moiré techniques can be correlated with appropriate control of variables [17]. Thus, the shadow moiré technique could be used for thermal warpage data and establishing average relative change data, even if DFP is used for production flatness measurements.

Conclusions

A potential approach to improve yield in the reflow assembly process is presented. The approach and data presented here is only a first phase concept, rather than a fully established solution for implementation. Further studies, using more realistic mating samples is the recommended next step. Further steps include, establishing conditions for acceptable interface gaps, further studying product warpage and production yield, communications with production equipment, and creation of production tools for warpage measurement of samples at room temperature.

Error in the prediction scheme is significant. The error here may come down with more realistic samples and larger product samplings. While the error is significant, the study also shows that the gaps between the samples at room temperature and at critical solder liquidus temperatures are noticeably different. Thus, using room temperature shape differences alone are not expected to provide the necessary information for selectively assembling component to board.

Strong control of product history and realistic reflow emulation in thermal warpage metrology will be essential to enable prediction of surface shapes at critical points in the reflow process.

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