Innerlayer Copper Balancing to Reduce PCB Surface Topography Under Large Form Factor BGAs

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Abstract
As CPU and GPU packages grow larger and contain higher pin/ball counts, the importance of managing the Printed Circuit Board (PCB) surface coplanarity for package assembly increases. The PCB surface coplanarity under a package is a product of both the global bow/twist of the PCB and the local surface topography under the package. In general, the surface topography is dependent the choice of material and layer stackup and the interaction between the innerlayer copper patterns and prepreg resin flow. This paper highlights key results from a HDPUG consortia project that evaluated multiple copper distribution strategies and their impact on surface topography across multiple materials and PCB fabricators. The work evaluated multiple package footprint sizes ranging from 26x26 mm to 100x100 mm, included eight different laminate materials spanning low to high flow characteristics, with multiple builds across eight (8) fabricators. This paper provides analysis of surface topography variations with respect to increasing package sizes due to copper balancing and copper distribution changes within a single layer, the stacking of copper patterns across layers, and the interaction with balancing resin fill rates between adjacent layers. Paper concludes with demonstrating that proper balancing of innerlayer copper and proper selection of material stacks can be used to manage surface topography requirements of large form factor packages.

Introduction
Advances in chiplet design and heterogeneous integration solutions in electronic packaging are enabling complex packages with increasing total die areas resulting in need for larger CPU and GPU packages [1]. Current CPU/GPU products such as Intel's Ponte Vecchio GPU and AMD's Genoa line of CPUs have package edge dimensions exceeding 75 mm. Based on trends and advances in package integration, it is expected that future packages exceeding 100-120 mm on a package edge will become more common. This increases the challenge of the Second Level Interconnect (SLI) assembly processes when attaching the package to the PCB due to the combined coplanarity and topography variations of the PCB and package. These combined influences between the PCB and package are the key drivers of SLI defects such as solder bridging or solder joint opens during PCB assembly [2],[3]. As the package X-Y dimensions increase, the sensitivity to package warpage and PCB coplanarity also increases. Figure 1 is a graphical depiction of how the global PCB warpage or curvature under the package must be smaller for larger packages to achieve the same PCB coplanarity under the package.

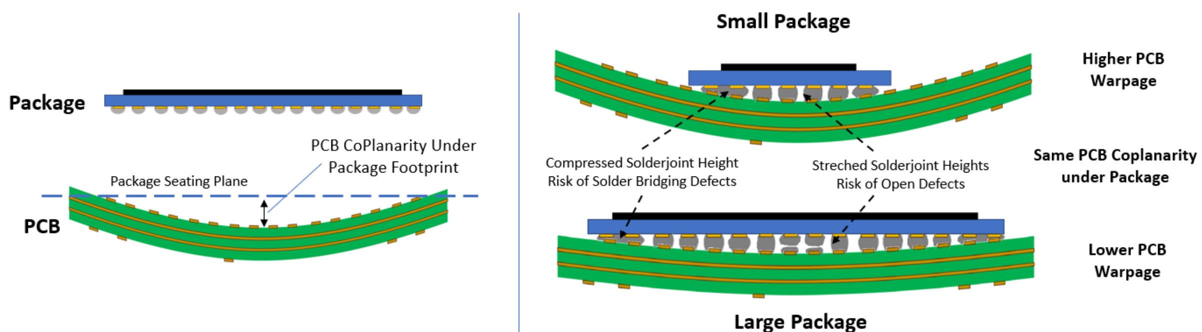

Figure 1 PCB Coplanarity Under Package

The characterization of PCB coplanarity under the package footprint has been studied and investigated for many years. Many works have investigated the influences of assembly temperatures on dynamic PCB coplanarity as the PCB and package move together through the assembly reflow temperature profile [4],[5],[6]. Other works have shown how the choice of PCB materials,

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** Based on results from High Density Packaging User Group (HDPUG) "Innerlayer Copper Balancing" Project

fabrication process conditions, and design each impact global PCB bow/twist and warpage [7]. In addition, it has also been demonstrated that the position within a single lamination press book can influence the observed PCB warpage and coplanarity. The difference by lamination book position is most likely due to the thermal lag between top/bottom of a press book and the middle of a press book.[2]. Most of these works have focused on global design or process metrics that characterize an individual PCB stackup or an individual PCB layer such as the resin CTE, selected glass construction of a prepreg or core, chosen copper thickness, or percent copper retained on an individual layer.

Global Copper Density and PCB Stackup Symmetry

It has also been noted through modeling and observation that PCB stackup symmetry is essential for both the thermo-mechanical properties and the thicknesses selection of materials, with respect to the neutral axis, to manage and minimizing PCB bow/twist and global warpage.[7],[8],[11]. There have also been published works on the impact of PCB fabrication process steps such as lamination or removal of copper through etching that impact PCB warpage [2],[8]. Figure 2 shows the ideal case of laminating two cores with prepreg. In this case the final thickness across a prepreg gap can be determined by the thickness of the copper on either side of the prepreg and the percent of retained copper on each layer. The evaluation of copper density (percent retained copper) across a manufacturing panel along with target dielectric thicknesses is used extensively in selecting prepreg thicknesses and resin content to generate a PCB stackup. Care is usually taken to balance the retained copper between centerline layer pairs across the centerline of a PCB, as shown in Figure 3, to prevent shifting of the PCB neutral axis that could initiate general warpage. Differences of 20-30% in 1oz copper layers can result in dielectric height differences of 6.4-9.6 um. While small, it can have noticeable impacts to the overall design, especially when a local difference is stacked across multiple layers within a stackup.

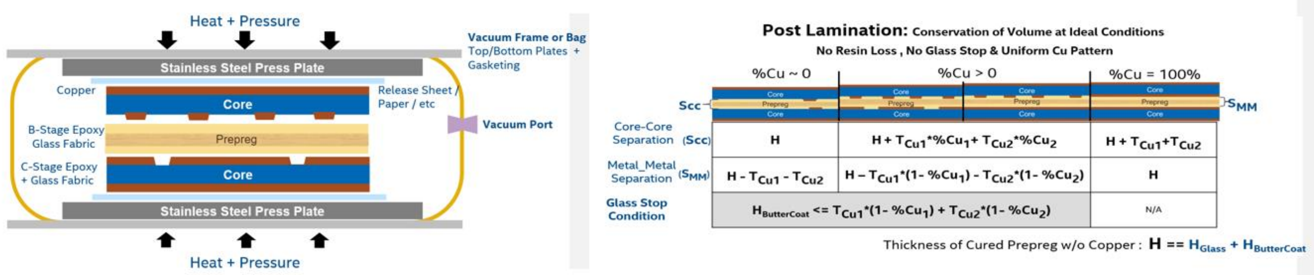
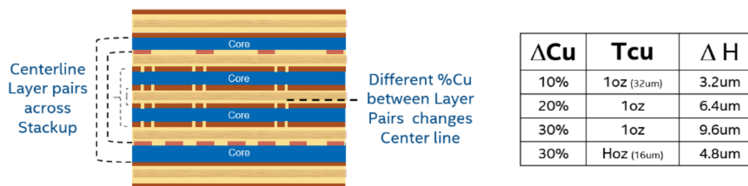


Figure 2 Lamination Process and Dielectric Separation Post Lamination



ΔCu	Tcu	Δ H
10%	1oz (32um)	3.2um
20%	1oz	6.4um
30%	1oz	9.6um
30%	Hoz (16um)	4.8um

Figure 3 Layer Pairs and Thickness Delta vs Delta Retained Copper

Local Copper Density under Package Footprint

While controlling global PCB bow/twist and warpage is important, it is the local PCB topography or coplanarity of the solder pads directly under an individual package that is critical in determining the SLI solderjoint. Prior work highlighted that localized variations of percent copper within an individual PCB layer can result in localized changes in prepreg thickness leading to core deformation [13]. Regardless of how well percent copper is balanced across centerline layer pairs, the percent copper directly under the package is usually much different that the average percent copper for an individual layer due to antipad arrays in plane layers or pad/trace density on signal layers as shown in Figure 4. The impact of these variations increases with higher layer PCB designs due to the repeating and stacking of these lower percent copper patterns across layers in the stackup. As noted in Figure 3, the usage of thick copper layers for power delivery also amplifies the impact of local copper variations as the copper void volume scales with copper thickness.

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For plane layers, there is usually a high density of via antipads under the package that locally decreases the percent copper compared with the area outside of the package footprint. For signal layers, the percent copper under the package is usually close to the percent copper outside the package footprint unless the design includes power/ground shapes for a mixed signal/plane design approach. Depending on design, this generally results in lower total copper volume under the Package footprint. Some work has been done to model the stresses profiles due to copper patterns within the PCB [12]. These modeling approaches help understand the impact of design; but they still rely on the assumption that the fabricated PCB layers have uniform thicknesses and that metal layers are not deformed and therefore sit within a fixed plane of the PCB.

Figure 4 Representative Retained Copper Outside & Inside a Package Footprint Area

PCB Surface Topography under Package

As the local total copper under a package is often different than outside the package footprint it is possible to obtain local thickness and surface topography variations across the PCB directly under the package driven by resin shrinkage during the lamination process [14],[15],[16]. Under packages with large edge dimensions or when using a resin with low flow characteristics there can be insufficient resin flow during the lamination cycle that can impact local PCB thicknesses and surface topography. Figure 5a shows the classical assumption where the PCB surfaces after the lamination process are planar with the press platen plates. Figure 5b shows the potential PCB cross-sectional deformation resulting from resin shrinkage. When the resin volume is uniform across the PCB, the impact of resin shrinkage is not noticeable as any resin shrinkage is also uniform across the PCB area. But, when the resin volume in not uniform across the PCB and not supported by PCB copper shapes, the impact of resin shrinkage will be proportional to the change in resin volume.

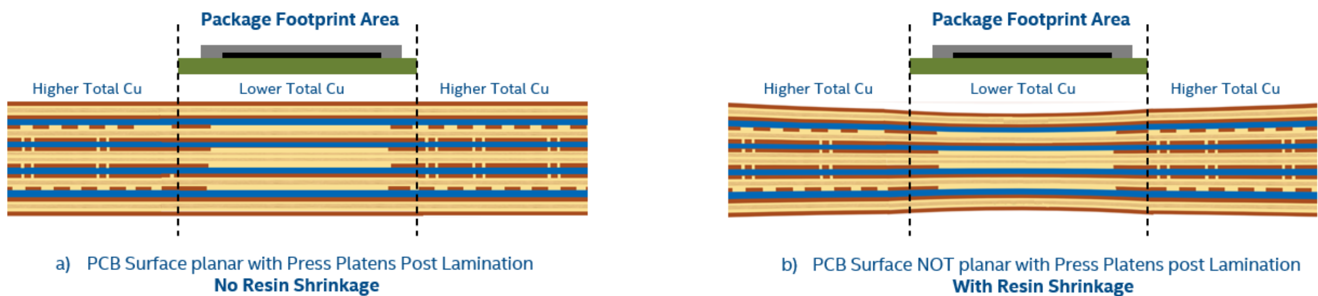

Figure 5 PCB Thickness Under Package with and Without Resin Shrinkage

Two types of resin shrinkage occur in a thermosetting resin during the lamination cure cycle [9]. The first is known as chemical shrinkage and is the volume reduction as result of crosslinking during cure. In lab measurements of general non-filled thermosetting resins, the chemical shrinkage has been characterized as a function of cure percentage with chemical shrinkage measuring around 7-10% at full cure [10], [14]. The use of fillers within the resin system would reduce the value proportionally to the filler volume with respect to a pure resin system. At this time, the chemical shrinkage data for the various resin systems used in common PCB laminates is not readily available. The second type of resin shrinkage is due to the coefficient of thermal expansion (CTE) and results during the cooling from the lamination cure temperature. While a CTE value can be obtained from PCB material datasheet, the reported value is based on a selected resin-glass composite using a specific glass style and resin content for resin. As such, the CTE shrinkage for local resin rich areas will be higher than reported on datasheets as the local area is filled with resin. While the mechanisms for chemical shrinkage and CTE shrinkage are different, the physical consequences are the same. As a result, several researchers have proposed simply modeling the combined result as an effective CTE. In a PCB composite stackup, the actual physical change in PCB thickness due to total resin shrinkage is also dependent the resin's ability to bend or compress materials within the PCB stackup based on their material modulus and thickness and the span of the resin rich pockets.

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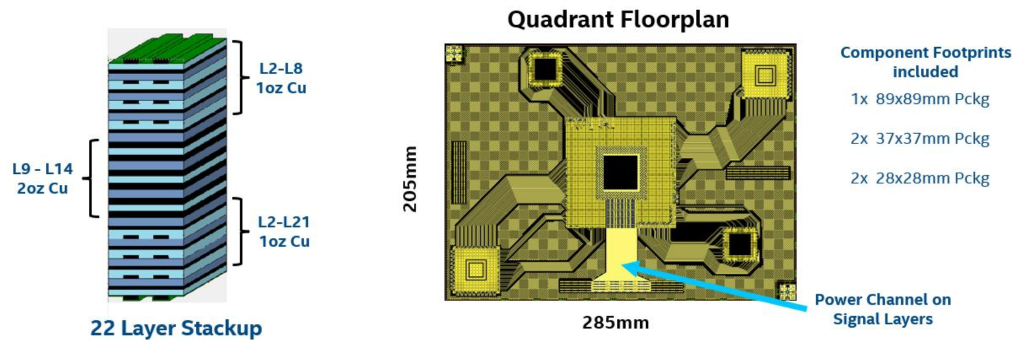
121
122 In some cases, under large package footprints, designers may stack power or shielding shapes which result in islands of higher
123 total copper within a local area under the package. In these cases, the mechanism of resin shrinkage could generate non-
124 standard profiles such as "W" shapes.
125
126 In the case of PCB prepreg selections with sufficient resin flow and available resin volume to fully fill regions with low retained
127 copper, it is possible to draw a conclusion that the PCB surface would be planar with the press platens at some point in time
128 prior to full cure with the resulting observed thickness reduction being solely due to resin shrinkage. But in the case of low
129 flow resins and/or PCB prepreg selection without sufficient available resin to fully fill regions of low retained copper, it may
130 be possible to generate PCB thickness and surface topography variations that are greater than that resulting from resin shrinkage
131 due to other mechanisms that generate core deformation [17].
132
133 Given the industry trends of larger packages and the resulting requirement to reduce PCB coplanarity of the package footprint,
134 the HDPUG consortia undertook an industry effort to evaluate the role of design and material selection on PCB coplanarity.
135 The goal was to study the relationship of PCB surface topography and coplanarity of the PCB package footprint to changes in
136 percent retained copper and the size of low/high copper areas within PCB. As newer electronic systems target ever increasing
137 data speeds and the usage of low loss and ultra-low loss PCB laminates increasing, the consortia effort also considered how
138 material selection impacted PCB coplanarity across different design conditions.
139
140 **Experimental Methodology**
141 A test vehicle was designed to evaluate a range of copper balancing distributions under various package footprint sizes ranging
142 from 28x28 mm to 89x89 mm. Figure 6 shows the test vehicle stackup and basic design floorplan. To drive a high range of
143 total copper and emulate high-end server and network systems, a symmetrical twenty-two (22) layer construction with target
144 2.50 mm final thickness was selected which consisted of six (6) layers of 2oz copper located at the center and six (6) layers of
145 1oz copper at the top and bottom of the stackup. The basic floorplan formfactor was 205x285 mm with a set of components
146 and connector placements. Component footprints included a large 89x89 mm footprint at 1mm pitch located at the center of
147 the floorplan, two 37x37 mm footprints at 0.8 mm pitch, and two 28x218 mm footprints at 0.65mm. A power channel from
148 the large package footprint was also included to replicate a common power delivery strategy of added copper fill regions on
149 signal layers. The component footprints were placed with large separations to minimize and potentially nullify interactions
150 between the copper variations of adjacent regions.
151



152
153 **Figure 6 Test Vehicle Stackup and Floorplan**
154
155 *Blocking for Manufacturing Factors*
156 The test vehicle design consisted of replicating the quadrant floorplan in a two-by-two grid to cover a full manufacturing panel
157 as shown in Figure 7. Each quadrant was designed with a different copper balancing strategy under the component footprints.
158 The copper patterns for an individual component footprint were identical for components replicated within a single quadrant.
159 The purpose of different copper balance strategies within the same manufacturing panel was to block out manufacturing process
160 and material lot factors. This approached allowed evaluation of design variations while maintaining the same press book
161 location, same lamination press load, same thermal profiles, and same physical core and prepreg.
162

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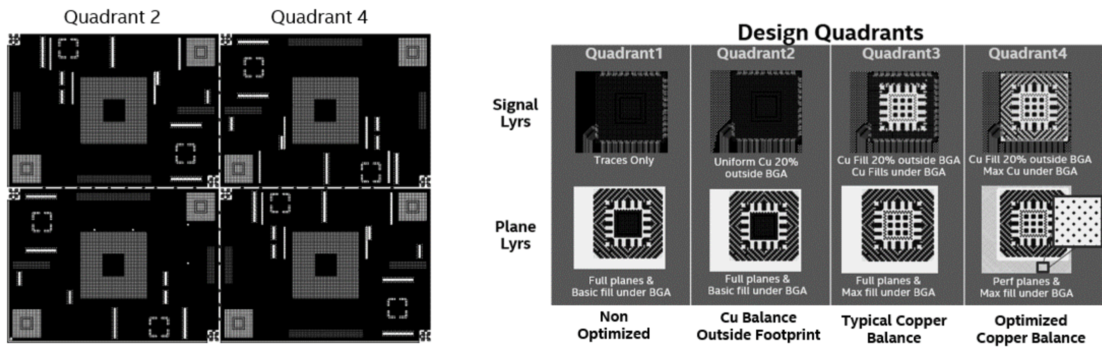
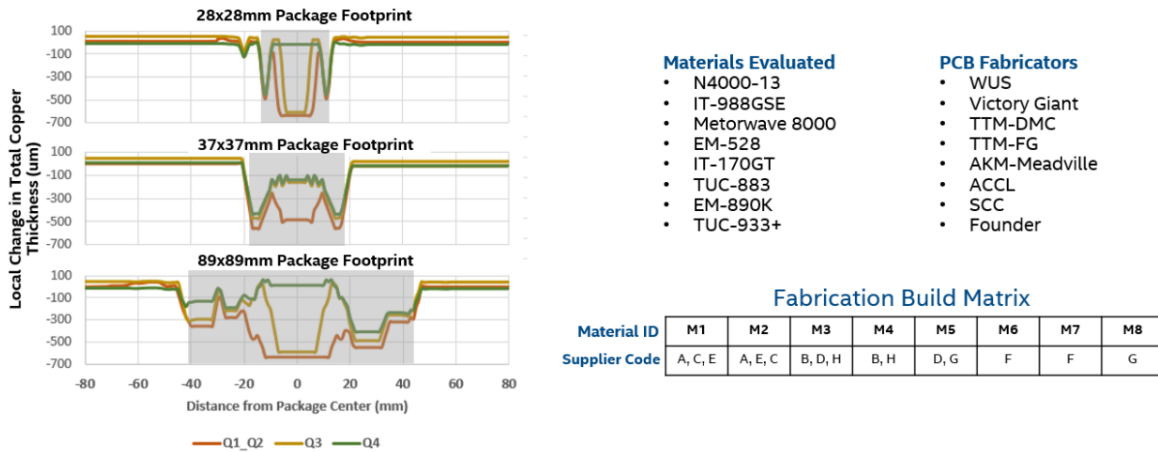


Figure 7 Full Test Vehicle Panel and Copper Balance Strategies by Quadrant

The copper balance strategy applied to each quadrant varied. A representation for a single layer and single component is shown in Figure 7. The copper balance strategy used in Quadrant 3 was set to mimic typical design approaches and copper fill percentages seen in typical designs. The strategy for Quadrant 4 was to maximize copper under the component footprint by selectively adding non-functional pads to power ground nets on specific layers and to add copper patterns on signal layers where possible to keep the percent copper uniform under the component. In some areas, achieving uniform percent copper included adding small voids or antipads to specific solid copper areas. Within Quadrant 4, care was also taken to ensure any open area under the component was filled, especially on thicker copper layers. Quadrant 1 and Quadrant 2 copper balance strategies that were selected to stress and test the limits and mechanisms of resin shrinkage and material resin flow across different void sizes and were not indicative of typical designs. The only difference between Quadrant 1 and Quadrant 2 was the inclusion of copper thieving outside the component footprints in Quadrant 2 to maintain a uniform 25% copper across the layer.

Fabrication and Material Scope

Eight (8) materials were included within the test to cover a reasonable sampling of traditional materials, low loss laminates and ultra-low low laminate materials. The test vehicle was fabricated across eight (8) supplier sites with each site completing two build lots with each build lot of a different laminate. In addition, five (5) of the eight (8) materials were replicated across two or three fabricators. See Figure 8. This approach provided good representation of fabricator-fabricator variance. Each fabricator selected the preferred core and prepreg combination to meet the target stackup.



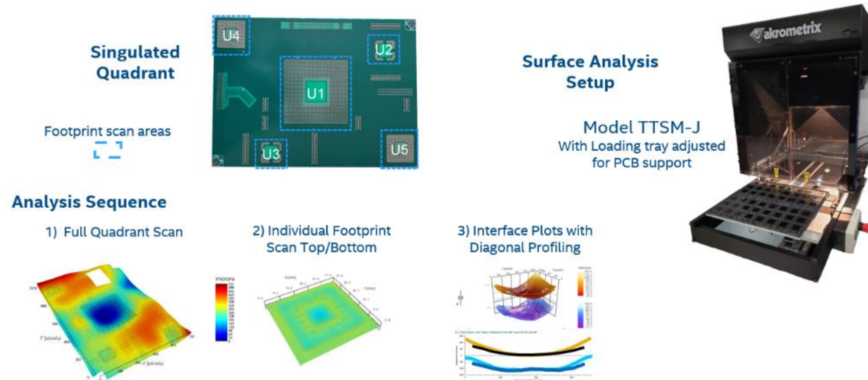
Material ID	M1	M2	M3	M4	M5	M6	M7	M8
Supplier Code	A, C, E	A, E, C	B, D, H	B, H	D, G	F	F	G

Figure 8 Build Matrix: Copper Distribution Profiles, Materials, and Fabricator Build Lots

Analysis Methodology

The warpage and coplanarity measurements were taken with shadow-moire technique at 1.7 um resolution using 150 line per inch grating. The tool model was an Akrometrix TTSM-J with the loading tray design adjusted for PCB support. For each build lot, four (4) manufacturing panels were selected, serialized, and singulated into the individual quadrants. The quadrant level warpage was first measured, then each of the five components footprints were measure both front and back. See Figure 9. The area of measurement for each component was 12.5 mm beyond the edge of the component perimeter. Analysis metrics of warpage and coplanarity were then obtained for front and back of each component footprint. Interface plots were also

195 obtained to evaluate local PCB thickness profiles along the diagonals of each component site in conjunction with the general
196 coplanarity of the site.
197

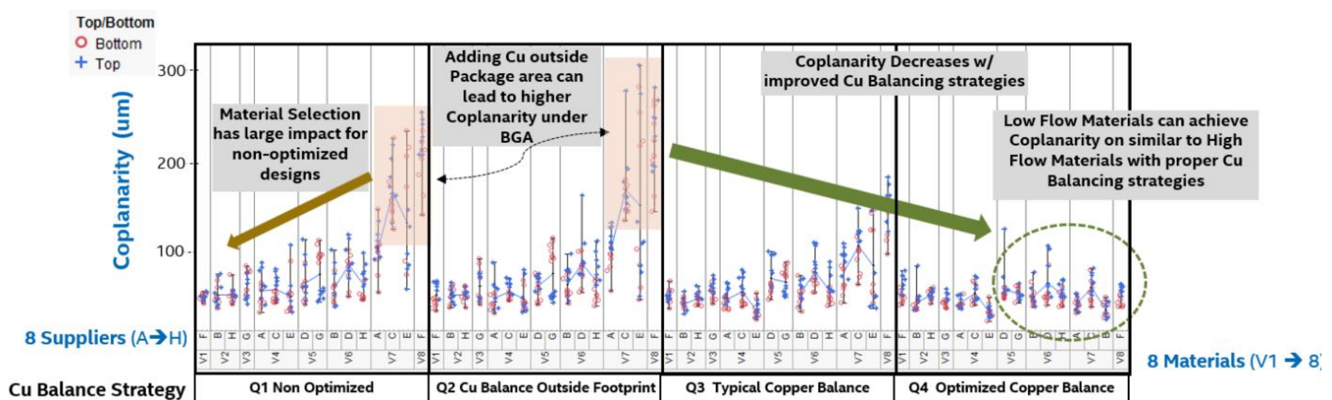


198
199 **Figure 9 Surface Analysis and Metrics**
200
201 Physical microsections were also taken after surface analysis by shadow moire. These microsections were done on a sampling
202 basis across different build lots, quadrants, and component sites to confirm PCB thickness variations obtained from the interface
203 plots. Measurements were taken every 1 mm along the microsection to generate profiles of PCB surfaces relative to the PCB
204 centerline. See Figure 10.
205

206
207 **Figure 10 Full Microsection Across Component Footprint**
208

209 **Results and Discussion**

210 The differences in copper balance strategies had a significant impact on the coplanarity under a component, even for small
211 package footprints. Figure 11 shows the measured results for the smaller 28x28 mm package footprint across the different
212 materials and PCB fabricator build lots. In Figure 11, the materials were ordered generically from highest to lowest resin flow
213 going left to right. First key observation was that the selection of material had a very significant impact when the design was
214 not optimized for copper balance. Whereas when the copper balancing was optimized, the choice of material had little impact
215 on average coplanarity with only a noted increase in variability for materials considered to be lower flow. This observation
216 matched general expectations based on the delta copper profiles for the 28x28 mm footprint as shown in Figure 8. The Q3
217 Typical Copper Balance condition had a smaller void region, and the Q4 Optimized Copper Balance condition had no center
218 void region.
219



220
221 **Figure 11 Coplanarity for 28x28 mm Package by Copper Balance Strategy, Material, and Fabricator**
222
223 Package size also had a significant impact on coplanarity. Figure 12 shows summary results of coplanarity for a selected high
224 flow, mid flow, and low flow material by package size and copper balance strategy. Each material in Figure 12 was fabricated
225 at multiple fabricators with data shown for the same material pooled across the fabricators. In general, for the same design
226 strategy and similar delta copper profiles under the component, the larger the package footprint the higher the average
227 coplanarity and the higher variation that was measured. This highlights that the need to optimize copper balancing for

coplanarity as package size increases. With optimized copper balancing, the coplanarity increased, but the difference between high flow, mid flow, and low flow materials was much lower. This demonstrates that sufficient copper balancing can enable the usage of lower flow materials – even with large package footprints.

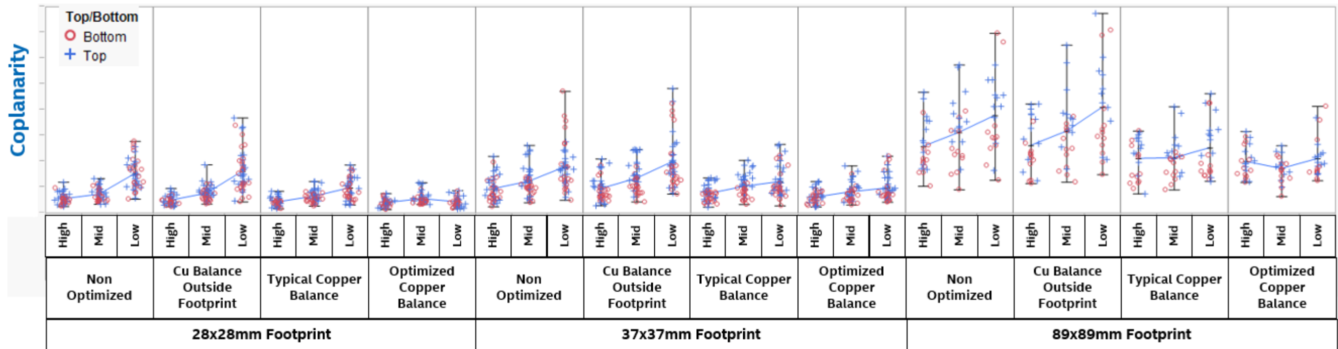


Figure 12 Coplanarity Difference between Higher & Lower Flow Laminates Across Package Size

Figure 13 shows the full data set of measured coplanarity across copper balance strategy, package footprint size, material, and PCB fabricator with respect to a 225 um coplanarity acceptance limit. It shows that with few exceptions small and medium sized package footprints can achieve low coplanarity requirements without much consideration for copper balancing. With larger package footprints, the need to balance copper becomes extremely critical.

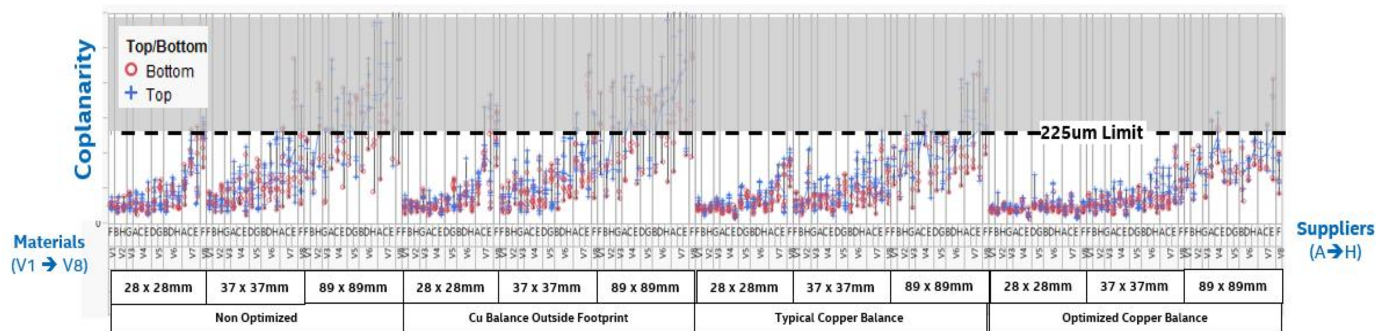


Figure 13 Measured Coplanarity by Copper Balance Strategy and Package Footprint Size

A key observation was that when comparing differences between PCB fabricators using the same materials, the coplanarity trends were the same and that the variation between PCB fabricators was small. It is important to note that the fabricators did not use the exact same prepreg glass styles or resin content which resulted in each fabricator having different levels of available resin volume for filling copper void areas under the component at each prepreg opening. Based on microsection analysis, this difference in stackup construction likely accounted for most differences seen between PCB fabricators rather than any differences in lamination profiles.

One unexpected result was that the measured coplanarity for quadrant Q2 was slightly higher than quadrant Q1 for some panels and some materials. The difference between the two design approaches was fairly minor. Q2 used the same copper patterns as Q1 quadrant except that a 25% copper thieving pattern was added to large areas outside of the component footprints that did not contain copper features. This was done on each of the six (6) 1oz signal layers to balance copper across the signal layers. See the representative signal and planes in Figure 14. This signal layer balancing was then maintained for both quadrant Q3 and Q4. In microsection analysis, the added copper outside of the component footprint was shown to have a higher measured PCB thickness around the outside of the component of 40-45 um as shown in Figure 14. This thickness change aligns with equations in Figure 2 when assuming an average 32 um thickness and an increase in the percent copper by 25% for each of the six 1oz copper layers.

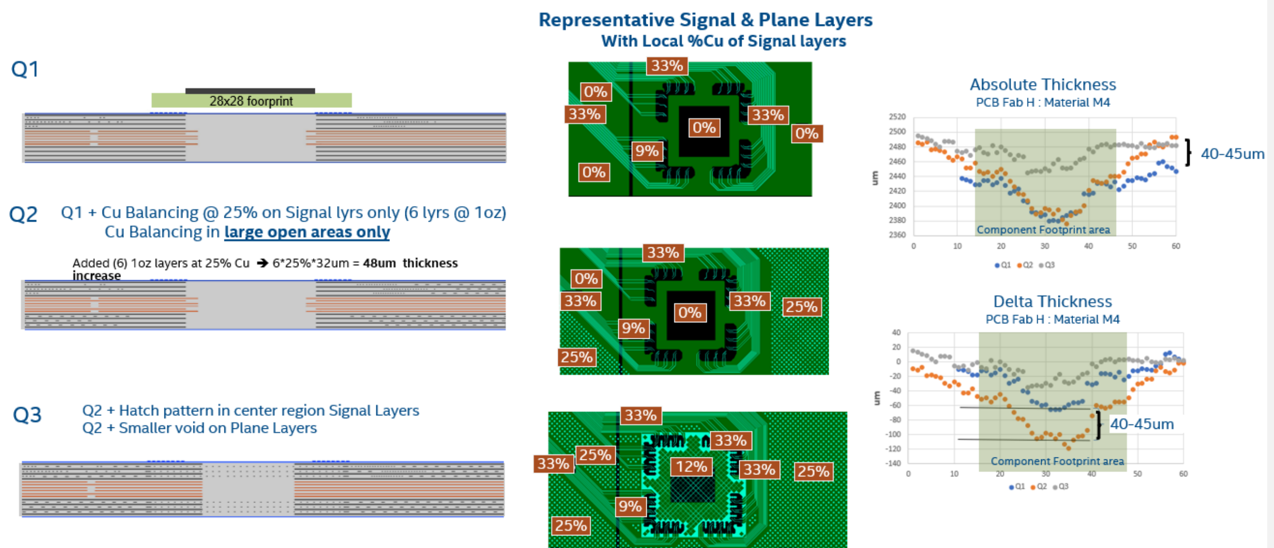


Figure 14 Representative Copper Distribution for 28x28 mm Footprint and Measured PCB Thicknesses

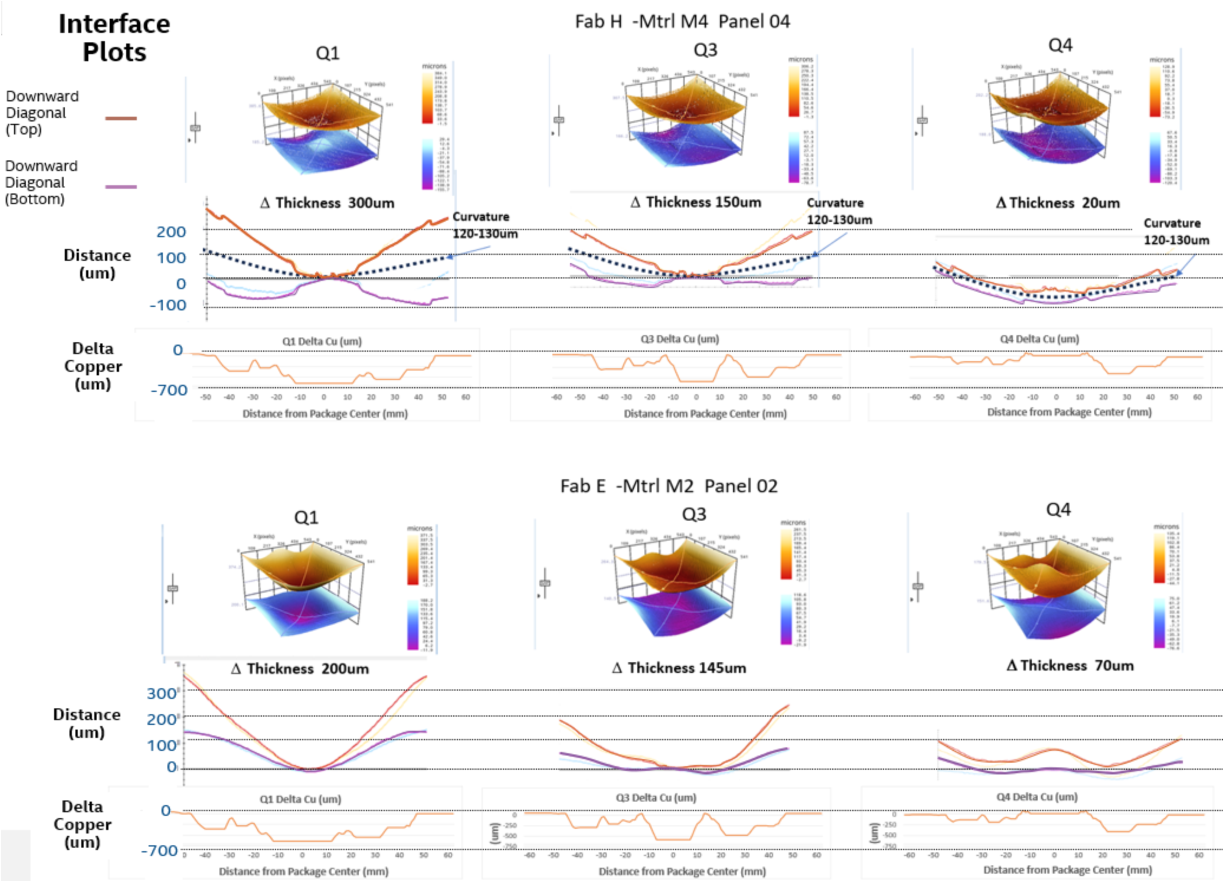
Another observation from the measured absolute thickness profile is that the thickness at the center of the component footprint of Q2 remained nearly the same as measured for Q1 even as the absolute thickness outside the component footprint increased. This is consistent as the copper profile under the component was identical for Q1 and Q2. As a result, the Q2 PCB surface had a larger delta thickness profile and a resulting higher coplanarity. In comparing Q1 and Q2 profiles across various materials, the distance from the component footprint at which the measured thickness increased by 40-45 um varied – most likely because of different flow characteristics. Lower flow materials showed the sharpest transition and higher flow materials a more gradual transition. This result also aligns with understanding of higher flow materials able to average out variations across a larger area.

For the footprint shown in Figure 14, Q3 maintained same copper profile outside the component footprint but added copper to the signal layers and reduced the copper void on plane layers under the component footprint. As expected, the absolute thickness outside the component footprint was also roughly same as Q2 with the thickness under the component increasing with the increased copper. Thus, Q3 had a reduced the delta PCB thickness across the component and consequently a reduced coplanarity relative to Q2 and Q1.

Coplanarity and Local PCB Thickness Variations

The data obtained from the Interface Plot feature in Akrometrix analytic software was used to separate the contribution of local PCB thickness variations and the contribution of bow/twist and warpage of the PCB on coplanarity of the component footprint. The interface plots also allow analysis of how the superposition of the two contributions resulted in coplanarity differences between front/back and between panels. The methodology of including different copper balance strategies within the same manufacturing panel made it possible to evaluate the progression of total coplanarity and local thickness variations as the profile of local copper changed. Figure 15 shows an example progression for different changes in local copper as well as the coplanarity and local PCB thickness for two different materials.

In the first example of Figure 15, Fab H – Mrtl M4 Panel 04, the curvature of the PCB at each of the panel quadrants was approximately the same at 120-130 um across the diagonal. The large delta copper void of Q1 resulted in a large thickness difference of 300 um between the center of the footprint to the outside of the footprint. In microsection analysis, this local delta thickness was shown to be very symmetrical around the centerline of the PCB. This local thickness variation was superimposed with the curvature to produce higher coplanarity on top and lower coplanarity on the back side. Due to the large thickness variation, the warpage (signed coplanarity) of the front and back side had the same sign. Moving to Q3, the magnitude of the delta copper void was slightly lower and smaller producing a local thickness delta of 150 um from the footprint center to the edge. The small thickness delta superimposed with the curvature reduced the backside to almost flat. In Q4, the delta copper void at center of the footprint was filled with copper. The resulting local thickness variation across the footprint was very small and the front/back coplanarity were nearly identical and tracked with the general curvature. Unlike Q1, the warpage between front and back of Q4 had opposite signs. In addition, as the local thickness was very small there was no evidence of a complex "W" surface profile as is expected from the delta copper profile.



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302 **Figure 15 Superposition of Local PCB Thickness Variations with General PCB Bow/Twist**

303

304 The second example in Figure 15, Fab E – Mtrl M2 Panel 02, also shows the superposition of the local PCB thickness and
305 general bow/twist and warpage. In this case, the local curvature of the PCB was different between the three shown quadrants,
306 but all had same general "Smiley" direction. The local thickness variations moving from Q1 to Q3 to Q4 reduced as the delta
307 copper was reduced. In this case, the Q4 the local PCB thickness across the component footprint followed the Delta copper
308 profile and resulted in a "W" thickness profile. This "W" thickness profile was superimposed to the general curvature within
309 the component footprint and resulted in a complex "W" surface topography. This "W" shape was evident in many of the larger
310 89x89 mm component footprint on specific materials and always followed in design conditions where the local PCB thickness
311 tracked with the delta copper.

312

313 Figure 16 shows multiple instances of the superposition of local PCB thickness profiles and various global PCB curvatures for
314 a few selected samples evaluated in this study. Figure 16 A1-A4 show instances of "Frown" global PCB curvatures and the
315 resulting different differences between coplanarity when measured from the top or bottom of the PCB. In the case of Figure
316 16-A2, the curvature negated the thickness variation resulting in a near flat surface on the top side, but the same location had a
317 high coplanarity on the bottom side. Figure 16-C2 shows the opposite result when the PCB curvature was "Smiley". The
318 superposition of the PCB curvature with a bow-tie thickness profile resulted in a variety of complex surface topographies.
319 Figure 16-C3 shows classical "W" profile on top with near flat on bottom side. Figure 16-A3 shows example of the bow-tie
320 profile appearing a be dominated by the PCB curvature so that the bottom side has no evidence of the bow-tie profile. Figure
321 16-A4 and B4 show that when curvature is small relative to the bow-tie profile variations that the surface topography can be
322 more complex than a simple "W" or "M" shape.

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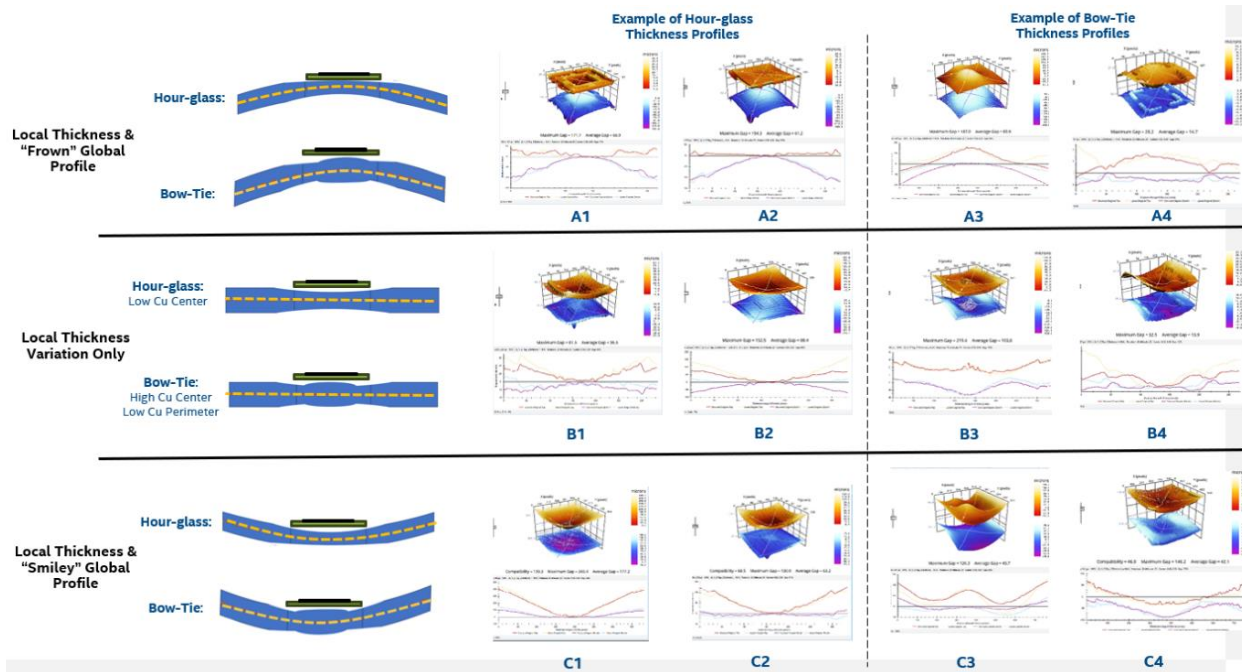

Figure 16 Local Coplanarity Examples of Local Thickness Variations Superposition with General PCB Bow/Twist

In general, there was no trend for general bow/twist curvatures by material, fabricator, or quadrant/design. There were observed panel to panel variations between "Smiley" or "Frown" curvatures within most fabrication build lots. For a given manufacturing panel, each of the quadrants behaved similar and had similar warpage signatures. The panel-to-panel differences should be investigated in a future effort as this has multiple potential contributors such as location within a press book, interactions with the singulation processes of the quadrants after arrival from fabricator, or handling of the individual quadrant units as shipped between physical locations for analysis and measurements.

The primary factors driving the local thickness variation at a given component footprint were the delta copper profile of each quadrant and size of the component footprint. The "hourglass" thickness shape always followed when the delta copper profile contained a high level of removed copper from the center. The "bowtie" thickness shape always followed when local areas within the interior of the component footprint had a region of max copper that approached or exceeded the copper outside of the footprint.

Figure 17 shows the relationship between local PCB thickness differences by the component footprints measured, different copper balance strategies and material selection. These measurements were obtained via Akrometrix interface analysis and confirmed with physical microsections on a random sampling. What is observed in Figure 17 is that the change in PCB thickness locally under each component had the same trends as the measured coplanarity across the various design and material factors seen in Figures 12 and 13. The magnitude of the local PCB thickness increased with component footprint size and was dependent on the material selection. In addition, there was a very strong correlation by design with the non-optimized designs having the highest delta thickness to the optimized copper balance designs having the lowest. And as noted in evaluating coplanarity, change as package footprint increased was smallest when using the optimized copper balance strategy.

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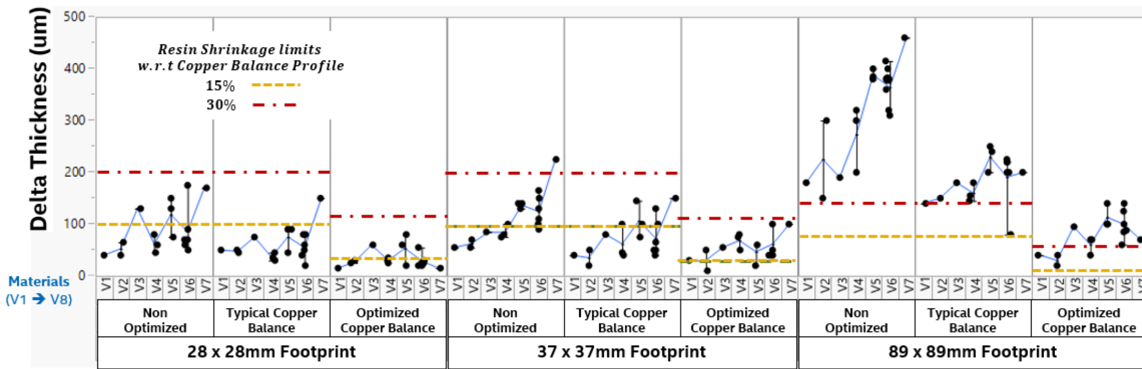

Figure 17 Delta Thickness under Component Footprint

As mentioned within the introduction, resin shrinkage due to chemical shrinkage and CTE shrinkage was expected to influence the local PCB thickness with respect to local changes in retained copper. Based on literature, it would be expected that the maximum contribution of resin shrinkage would be less than 12-15% of the total local change in copper. Based on mechanism of resin shrinkage, it was only expected to significantly contribute where there existed larger areas devoid of copper. The Resin shrinkage limits shown in Figure 17 reflect the differences in both percent copper and void size for each of the three design strategies. As seen in Figure 17, a 15% resin shrinkage would not encompass the magnitude of thickness changes measured. Even increasing the expected resin shrinkage to 30% was not sufficient to explain the measured thickness changes.

In addition, materials that contained fillers were expected to have a reduced contribution from resin shrinkage. In general, the measured data showed that the filled materials had a higher thickness change which is counter to the expectation for these materials. A key hypothesis from this data is that resin shrinkage is not the driving factor of the larger local thickness changes in this study. This implies that the PCB top and bottom surfaces had the topography variations locked in during the lamination cycle and that the surfaces should not be assumed to have been planar with the press platens at the final stages of cure. This opens additional questions and future investigations of local surface topography variations during and immediately after the lamination press process and the role of resin flow, innerlayer core deformation during lamination, and selection of individual prepreg styles.

The correlation of coplanarity to the local PCB thickness variation was evaluated by plotting the combined total of top and bottom coplanarity at each component footprint site against the measured thickness variation at the same location as shown in Figure 18. In this analysis all fabricators and materials were combined. In addition, all component footprint sizes were pooled. The top and bottom coplanarity were combined into a single composite value to normalize superposition of the global curvature as the global curvature would increase coplanarity or one side and decrease the coplanarity on the opposite side.

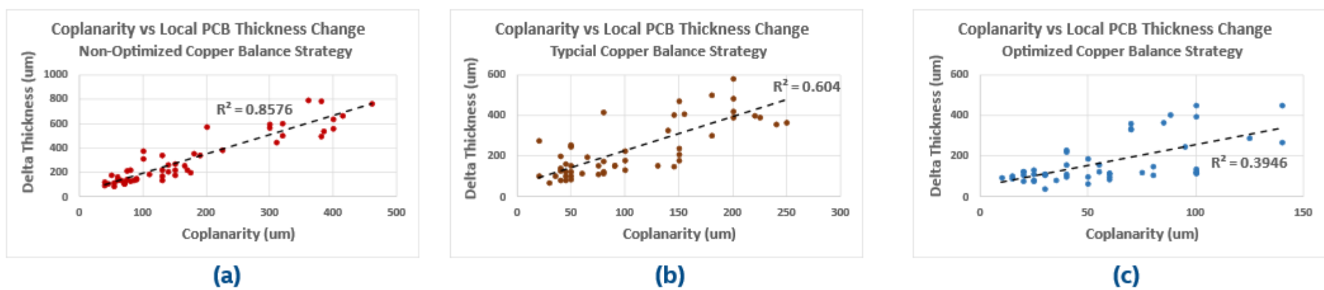

Figure 18 Coplanarity (Top + Bottom) vs Local Delta Thickness and Copper Balance Strategy

The trend of coplanarity with respect to changes in local PCB thickness were positive across all copper balance strategies. The highest correlation R value was with the non-optimized copper balance strategy. The R value decreased as the copper optimization was improved. This follows expectation and experience as other factors become more dominate as the local copper is balanced across the component footprint.

Conclusions

*As originally presented at IPC APEX 2024.

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384 It was shown in this study that design and material/stackup selection can be the primary factors influencing coplanarity variation
385 under a component. It was also demonstrated that for the same copper balance strategy coplanarity increases as the component
386 footprint dimensions increase.
387
388 The profile of retained copper under a component has a direct relationship with the surface topography and coplanarity variation
389 of the PCB footprint for the component. It was shown that as the total removed copper increases, the coplanarity increases.
390 This could be due to the PCB stackup either increasing layers of copper or using thicker copper with the same antipad and fill
391 patterns. As silicon substrate packages grow size it is increasingly important to balance the percent of retained copper under
392 the package footprint and match it to the percentage of copper outside the package on each layer and balance the total across
393 layers.
394
395 Large reductions in total copper under a component footprint leads to an hourglass PCB thickness profile and can be a major
396 driver of high localized PCB coplanarity variations under components. Generally, this is result of having a high concentration
397 of antipads, or incomplete copper floods on power layers under a component resulting in a change in percent retained copper.
398 The impact grows proportionally higher with more and/or thicker copper layers. This can be optimized by selective adding
399 non-functional pads for power and ground nets and fill any open areas on both signal and plane layers. Care should be taken
400 when using mixed signal/planes on an individual PCB stackup layer as stacking localized areas of high copper under the
401 component footprint can result in complex "W" or "Bowtie" surface profiles that add complexity to the Second Level
402 Integration of the package and PCB.
403
404 The selection of materials in a PCB stackup can impact the variability and average coplanarity within a given design, especially
405 as component dimensions increase. The impact of material selection is much less when the design is optimized for copper
406 balancing. Basically, it is very difficult to correct a poor design that has high copper imbalance through either material selection
407 or process.
408
409 While resin shrinkage is real and is a consideration for local variations in larger resin pockets, it was shown that it is not likely
410 the driving vector in cases of high coplanarity variation under a component.
411
412 The usage of interface analysis obtained by scanning top and bottom surfaces of the PCB, such as the Akrometrix method, can
413 be used to quantify and differentiate the contribution of local PCB thickness variations and the global PCB bow/twist or
414 warpage on the coplanarity at a component footprint. The high correlation of coplanarity to local PCB thickness variations
415 across materials and copper balance strategies provides an opportunity for designers and PCB fabricators to gage the 'goodness'
416 of a design and material selection by evaluating the local PCB thickness profile. By combining the technique with analysis of
417 the total retained copper profile outside the component footprint and under the component footprint it is possible to determine
418 where and how copper balancing improvements should be implemented. This can also be used to prioritize between design
419 changes or material choices vs process changes when addressing coplanarity issues.
420
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427
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