PCB WEST 2017
Conference & Exhibition

VARIABLES AFFECTING BARE PCB WARPAGE DURING REFLOW; A STUDY ON SUPPORT METHODS AND TEMPERATURE UNIFORMITY

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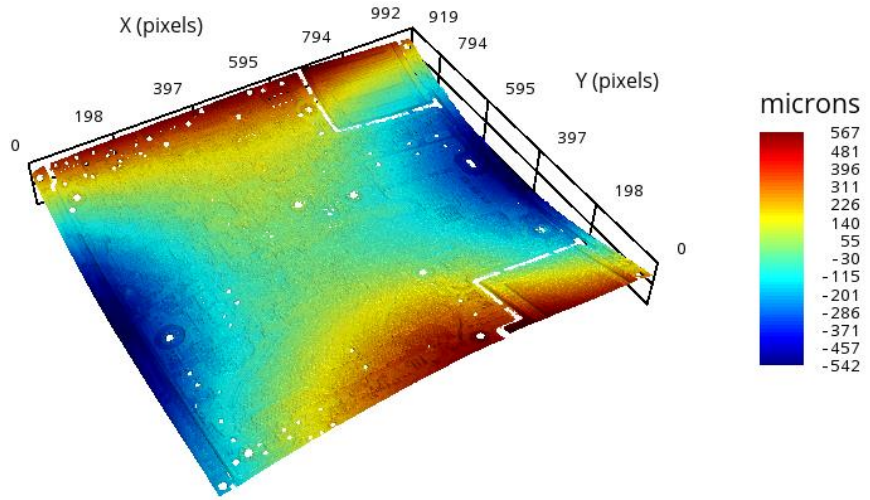
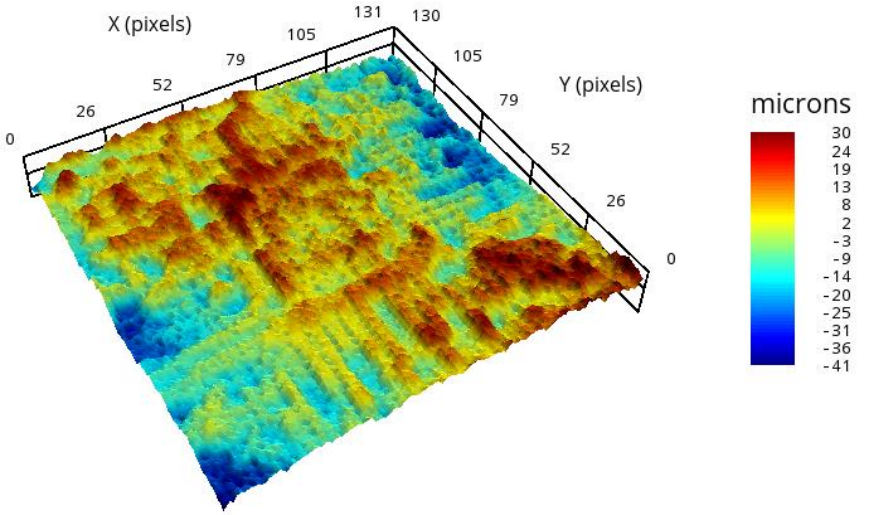
Overview

- PCB flatness over temperature is a critical factor for reliable SMT
  - Industry studies and standards provide context
- This study does not cover PCB design variables that affect warpage
- The study focuses on variables of the reflow process that affect PCB warpage
  - Temperature Uniformity (hot leading edge)
  - Sample Support Method





Agenda

- Background of Industry Standards Relating to PCB Warpage
- Background of PCB Warpage Studies
- Conceptual Points
- Case Study Test Plan
  - Controls and Variables
  - Hypothesis
- Case Study Results
- Lessons Learned
- Potential Future Work

Related Industry Standards

- IPC-A-600, IPC-6012, IPC-2221, IPC-7095 – Multiple IPC standards that have been updated over time
  - Update established Bow and Twist less than 0.75% for PCB with surface mount and 1.5% for PCBs without surface mount
- IPC-TM-650 2.4.22C - Test Methods Manual - 1999
  - Procedures to measure bow and twist of a PCB
- IPC-9641 – High Temperature Printed Board Flatness Guideline - 2013
  - Methodology for measuring PCB flatness over reflow profile
  - Focuses on warpage of areas with surface mount attach
  - Doesn’t establish pass/fail criteria

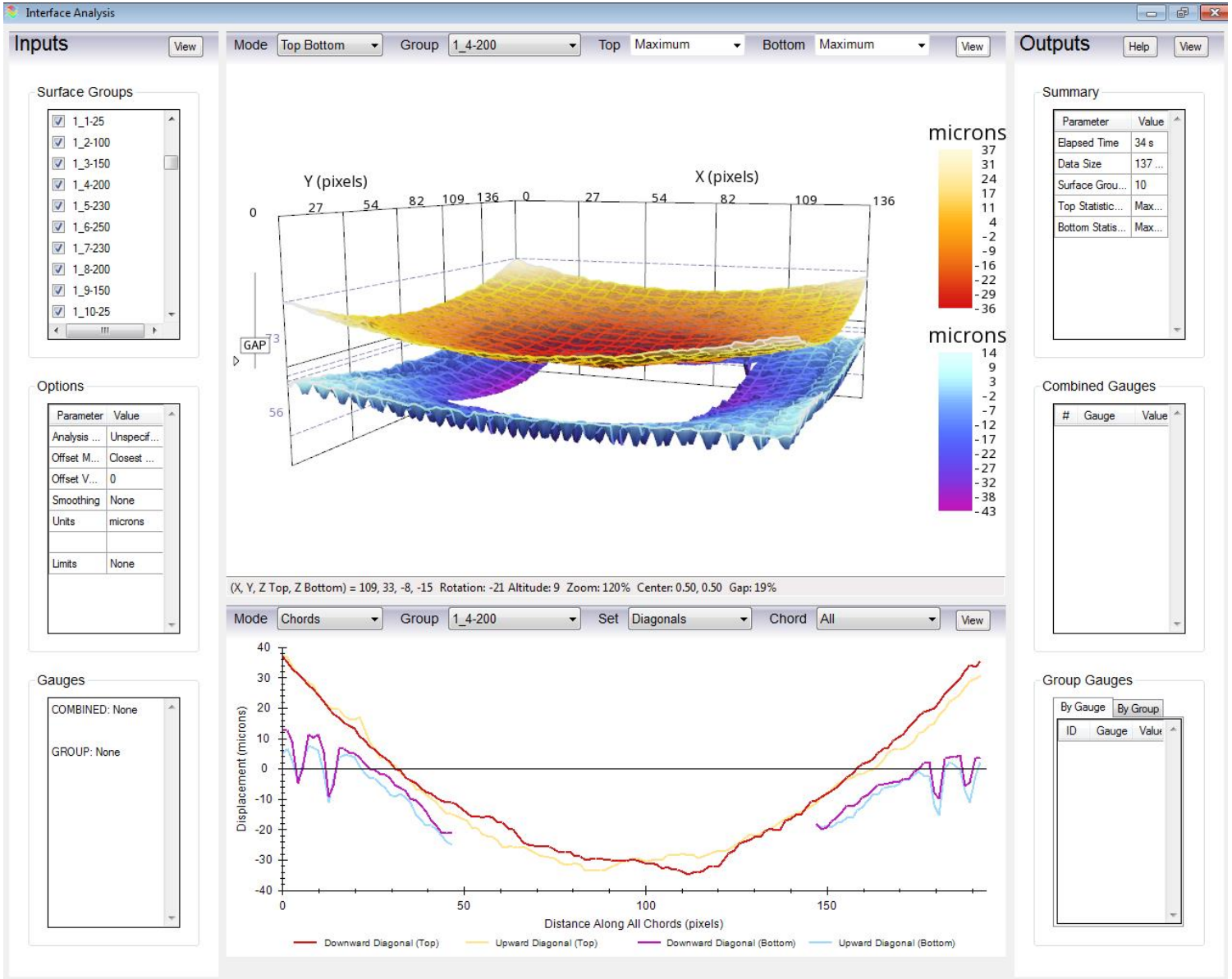
Thinking Globally, Measuring Locally

- "Thinking Globally, Measuring Locally" published in *Printed Circuit Fabrication* in 1998 (IPC-9641 in 2013)
- From JEITA-ED-7306 - Measurement methods of package warpage at elevated temperature and the maximum permissible warpage
  - "Maximum permissible package warpage of BGA is given 80 % of the maximum relative displacement that does not cause open solder joints or solder bridges. The other 20 % of the displacement is reserved for a tolerance of the PWB warpage and the fluctuation of the paste thickness."
  - Includes pass/fail standards for BGA/LGA side of attach
    - Theoretically gives a reference for local area PCB warpage, assuming all of the 20% is reserved for PCB warpage
  - Similar to JEDEC JESD22-B112A

Thinking Globally, Measuring Locally – Industry Drivers

- How big are server packages going to get and at what solder ball pitch/size?
  - Typically, thicker boards will help local warpage levels
  - Packages covering larger areas will more sensitive to PCB warpage
- How thin will mobile device substrates be?
  - Typically leads to higher warpage levels
  - Often matched with small, thin, tight pitch packages
- Is dual surface analysis feasible?
  - Individual warpage standards are not needed if warpage data is consistently available between two mating surfaces
  - If feasible, standards would shift toward a dual surface gap specification based on ball/land size/pitch

Dual Surface Analysis



Industry Studies

- 1997 *Electronics Engineer* Magazine - “Controlling Bow and Twist”
- 2001 Pan Pacific “Advanced Warpage Characterization: Location and Type of Displacement Can Be Equally as Important as Magnitude”
- 2003 SMTA International – “Effect of Printed Wiring Board Warpage on Ball Grid Arrays Over Temperature”
- 2003 EPTC - “New Package/Board Materials Technology for Next-Generation Convergent Microsystems”
- 2004 Pan Pacific - “Correlation of Solder Joint Reliability of µPGA Socket to Package Flatness and PCB Warpage”

Industry Studies in Detail

- "PCB Dynamic Coplanarity at Elevated Temperatures" (iNEMI) – SMTA International 2011

Key Message

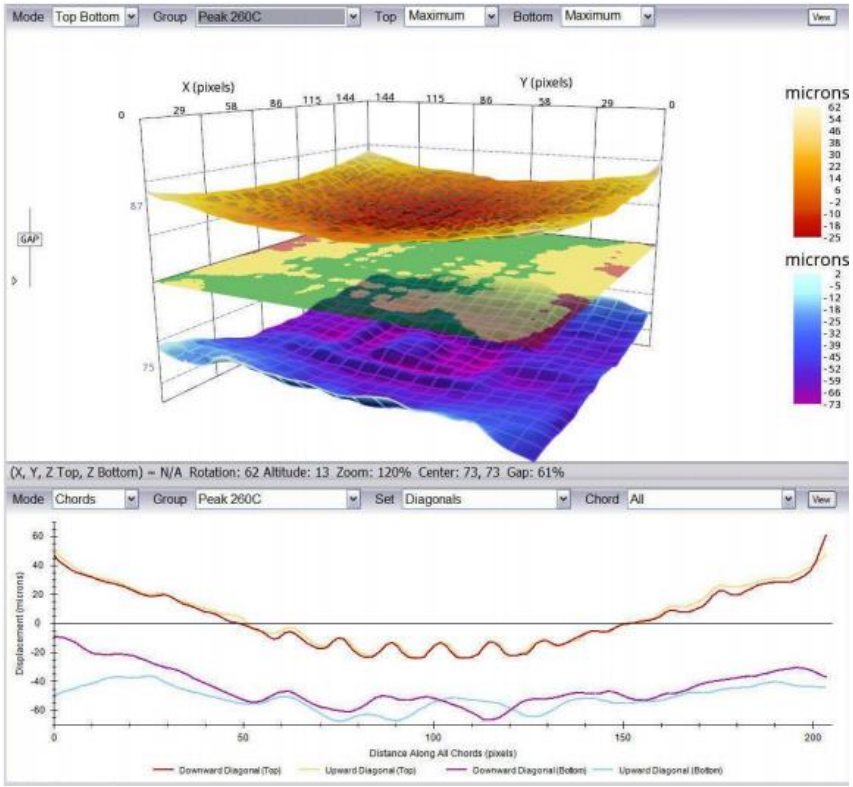
- Shadow moiré is a viable test methodology for determining dynamic coplanarity values
- Design of PCB/BGA area appears to be the largest factor in coplanarity
  - Thinner PCBs have higher warpage than thicker PCB
  - Variance within a single lot of PCB is often over 50%

Summary

- WG recommends IPC to review warp & twist and bow test methodology and develop one that includes BGA or local area of interest
- WG recommends that IPC and JEDEC to format a joint evaluation WG to jointly set the requirements for board and package
- WG recommends a study of PCB fabrication/processes influence to quantify the warpage impact

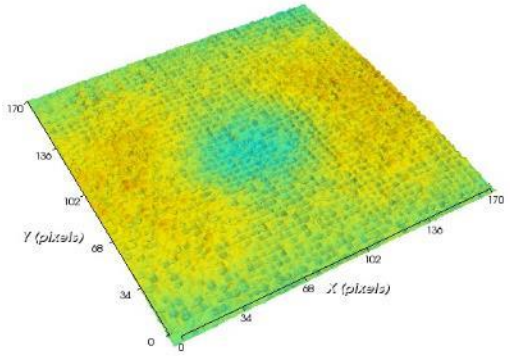
Industry Studies in Detail

- "Advanced Second Level Assembly Analysis Techniques - Troubleshooting Head-In-Pillow, Opens, and Shorts with Dual Full-Field 3D Surface Warpage Data Sets" IPC APEX 2013
  - Details how PCB and BGA attach surfaces can be match together
  - Focused on potential solution the Head-in-pillow (HiP) issues



Industry Studies in Detail

- "Surface Mount Signed Warpage Case Study; New Methods for Characterizing 3D Shapes Through Reflow Temperatures" IPC APEX 2017
  - Focused on surface mount packages but raises questions that would need to be answer for PCB local area warpage
  - Proposed alternate gauge and shape name solutions
  - If making decisions based on PCB warpage coplanarity, bow, and twist may not be effective
    - Issues related to local surfaces features detailed later



FullFieldSignedWarpage = 99 microns

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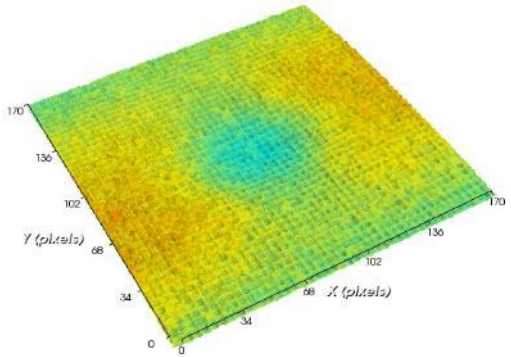
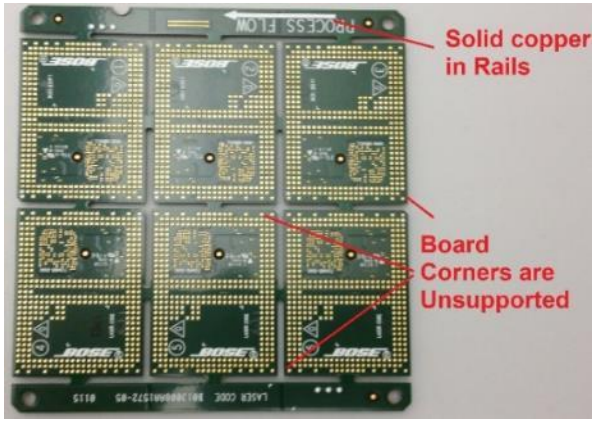
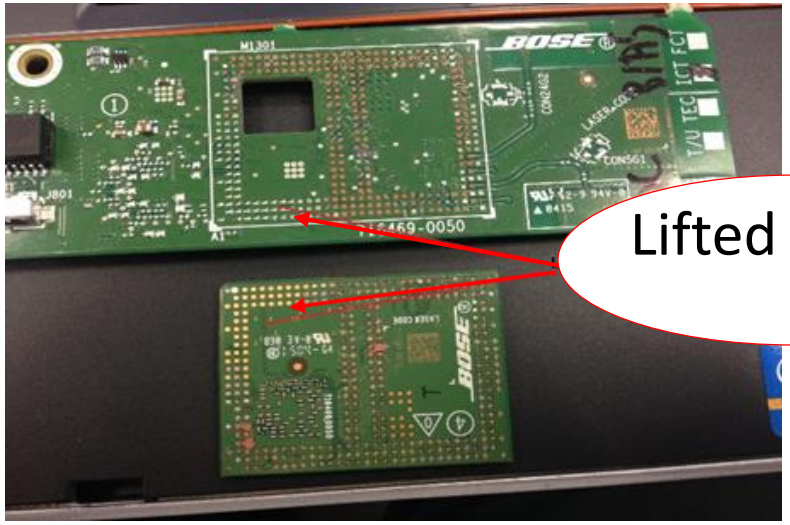


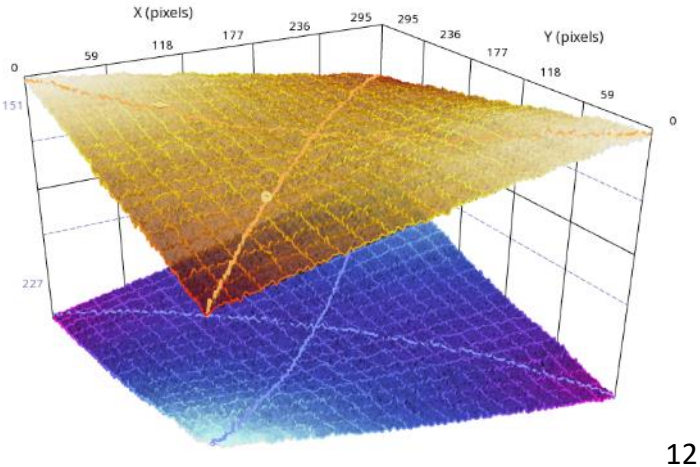
FullFieldSignedWarpage = -103 microns

Industry Studies in Detail

- "Understanding PCB Design Variables that Contribute to Warpage During Module-carrier Attachment" SMTAI 2016 (Bose paper)
- Corner of mating surface is not soldered
- 50,000 ppm defect rate needs to be reduced
- Effort needed to try and determine
  - Material, design, and process factors







Bose Paper - Phase 1

- How does coplanarity of module and panel correlate with failures?
- Phase one of the experiment measured the full population of PCBS in groups A, B and C before and after top-side assembly

Phase 1

Sample Allocation (by individual circuit and 6-up panel)

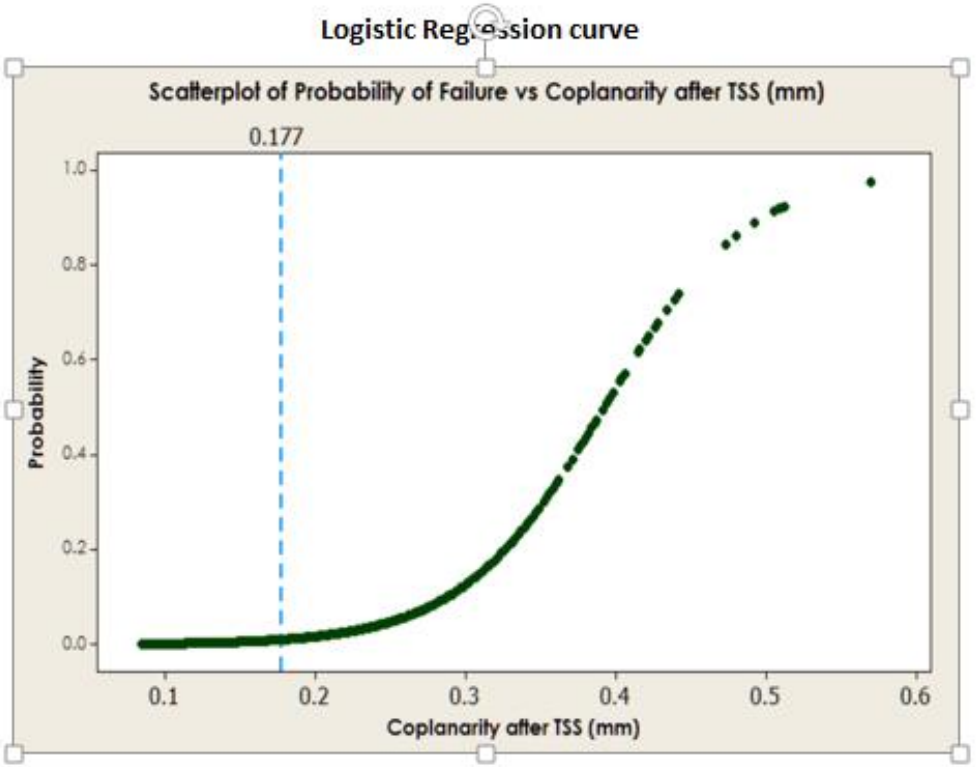
	Modules		Panels (6-up)	
Group	**Supplier A**	**Supplier B**	**Supplier A**	**Supplier B**
A Warp <0.5mm	1380	1380	230	230
B Warp >0.5mm, ≤1mm	1380	1380	230	230
C >1.0mm	438	726	73	121
TOTALS	**3198**	**3486**	**533**	**581**

Bose Paper - Phase 2

- Phase two of the experiment involved the same measurement strategy as phase one using PWBs and implementing the material and design changes the team wished to investigate. Attributes to be studied included:
  - Materials
  - Working panel position
  - Copper content of the rails
  - Board break quantity and position
  - Copper balance
  - Supplier

Bose Paper - Phase 1: Results

- Statistical failure probability



- 1.08% failure rate at .177mm coplanarity

- Pass/fail percentages based module position in panel

Board Position Contingency Table

		Pass	Fail	Total
Board 1	Row count	785	16	801
	Row percent	98	2	100
Board 2	Row count	785	16	801
	Row percent	98	2	100
Board 3	Row count	789	12	801
	Row percent	98.5	1.5	100
Board 4	Row count	784	17	801
	Row percent	97.88	2.12	100
Board 5	Row count	790	11	801
	Row percent	98.63	1.37	100
Board 6	Row count	784	17	801
	Row percent	97.88	2.12	100
Total	Row count	4717	89	4806
	Row percent	98.15	1.85	100

Pearson Chi-Square = 2.393, DF = 5, P-Value = 0.793
Likelihood Ratio Chi-Square = 2.496, DF = 5, P-Value = 0.777

Bose Paper - Phase 2: Results

- Pass/fail between corner boards –vs – non corner boards

Working Panel Position Contingency Table

		0	1	
		Pass	Fail	Total
Corner boards	Row count	512	16	528
	Row percent	96.97	3.03	100
Non corner boards	Row count	2680	20	2700
	Row percent	99.26	0.74	100
Total	Row count	3192	36	3228
	Row percent	98.88	1.12	100

Pearson Chi-Square = 20.993, DF = 1, P-Value = 0.000
Likelihood Ratio Chi-Square = 15.855, DF = 1, P-Value = 0.000

- Pass/fail between current corner tabs and extra tabs in corner

Break Tab Contingency Table

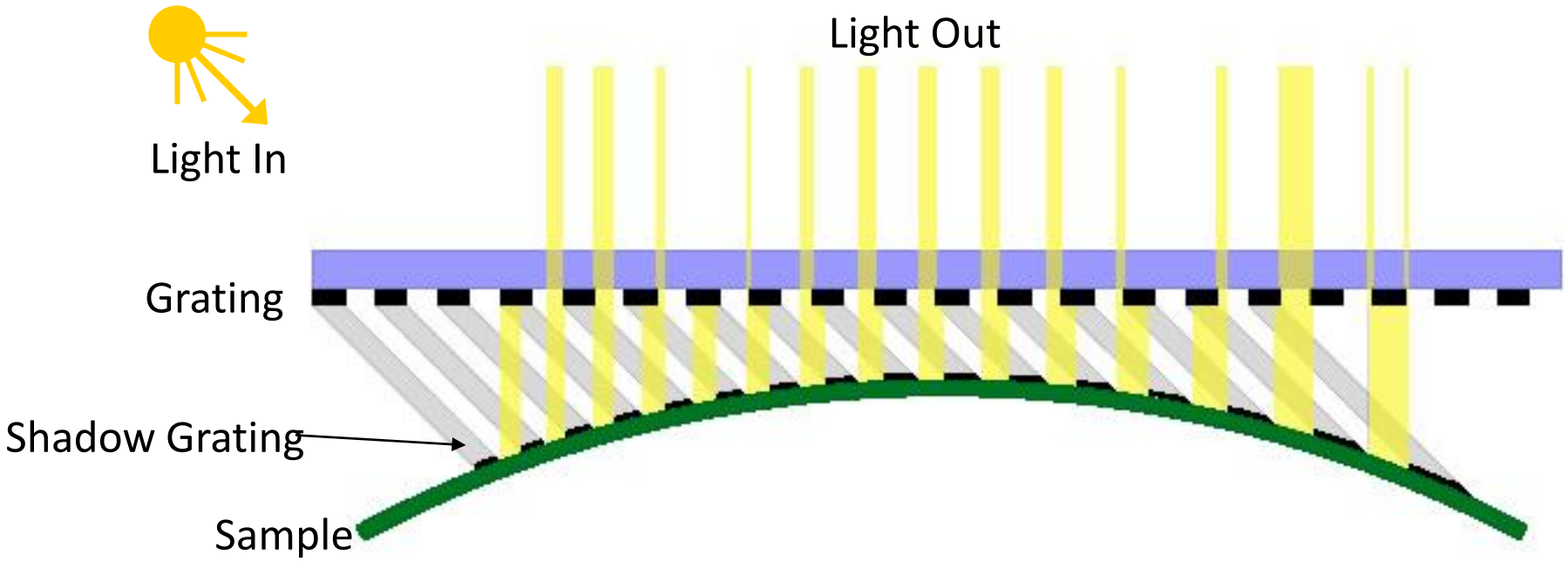
		0	1	
		Pass	Fail	Total
Current tabs	Row count	2586	36	2622
	Row percent	98.63	1.37	100
Extra tabs	Row count	606	0	606
	Row percent	100	0	100
Total	Row count	3192	36	3228
	Row percent	98.88	1.12	100

Pearson Chi-Square = 8.414, DF = 1, P-Value = 0.004
Likelihood Ratio Chi-Square = 15.064, DF = 1, P-Value = 0.000

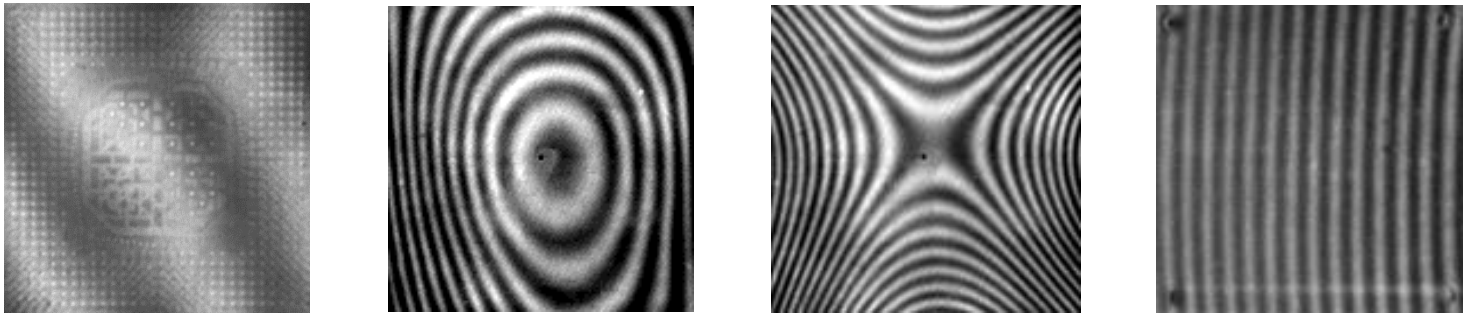
Industry Studies in Detail - Upcoming

- "Approaches to Minimize PCB Warpage in Board Assembly Process to Improve SMT Yield" – Early phases
  - Identifies a lack of industry spec for PCB warpage at room and elevated temperature
  - Focus on board thickness, Cu balance, lamination process, outrigger design and tabs, PCB location in panel and panel size, pallet design and material, etc.
  - Not intended to establish a warpage specification
- Untitled paper from MTC (Manufacturing Technology Center) in the UK – Early phases
  - Focus on reflow profile, laminate material, board thickness
- And likely many more studies… Questions?

Concepts - A Brief Explanation of the Shadow Moiré Technique

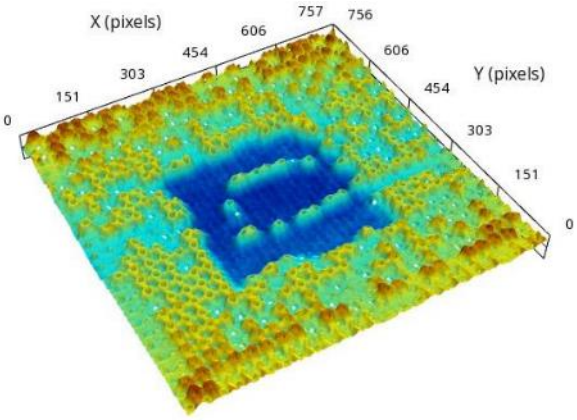


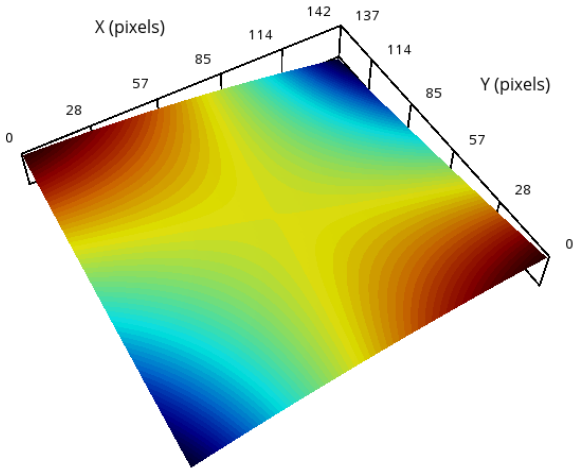
Example Fringe Intensity Images



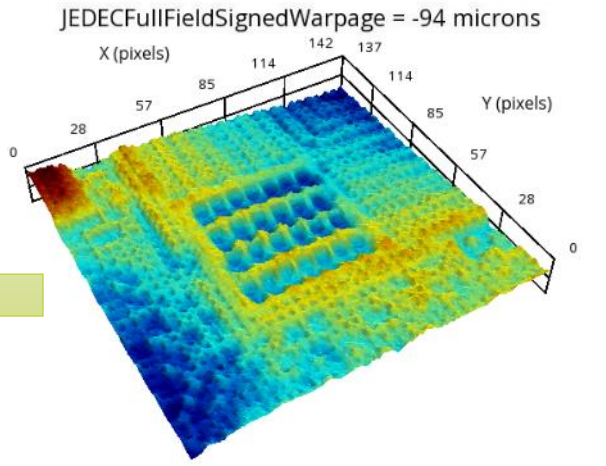
Concepts – PCB Locals and Surface Features

- Coplanarity of surface mount attach areas on PCBs is often largely influenced by local features
- Features can significantly affect coplanarity, bow and twist
- Local features often too large for smoothing effects to be viable; polynomial surface fits may be better solution
- New gauges based on overall curvature may also be needed (3S/SS)





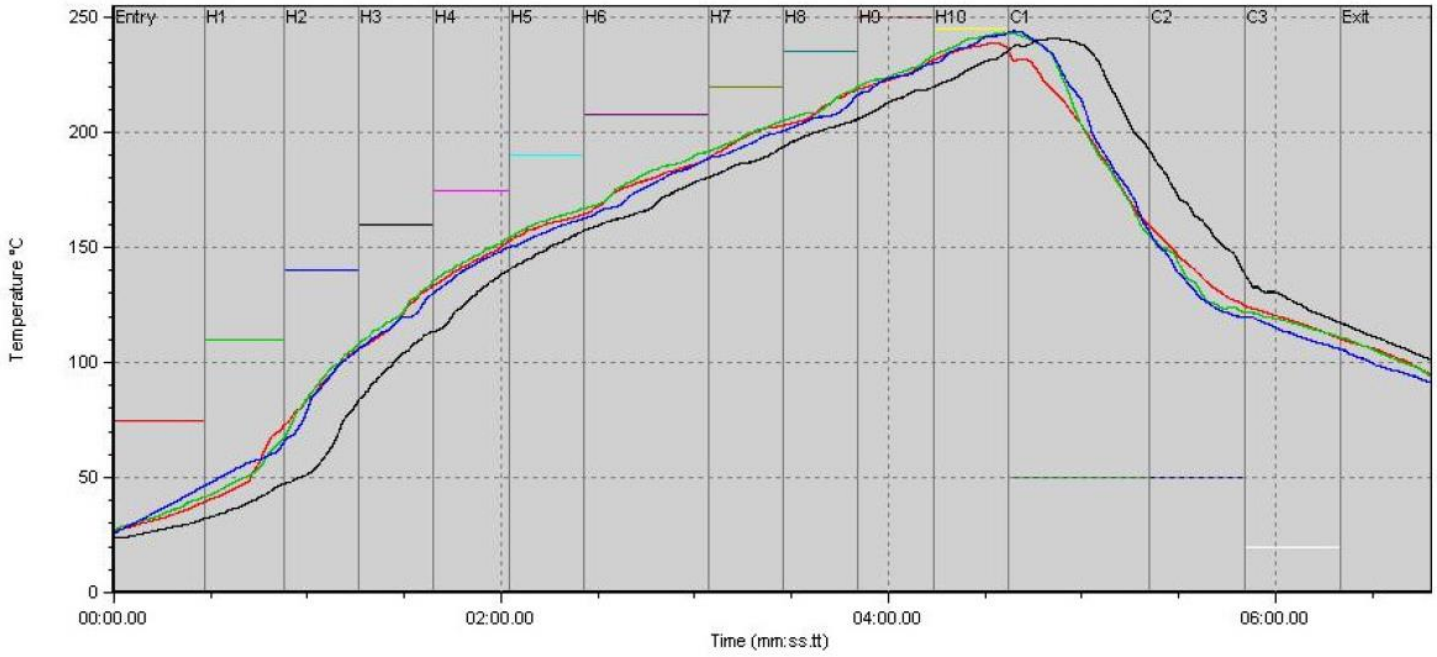
Coplanarity = 59.8 microns



Coplanarity = 93.8 microns

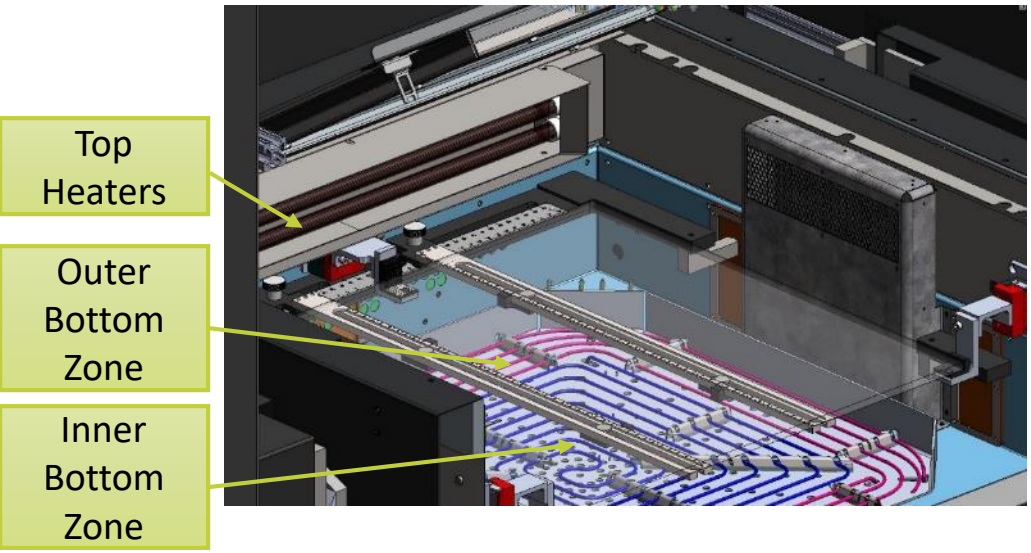
Concepts – Reflow Ovens, Hot Leading Edge

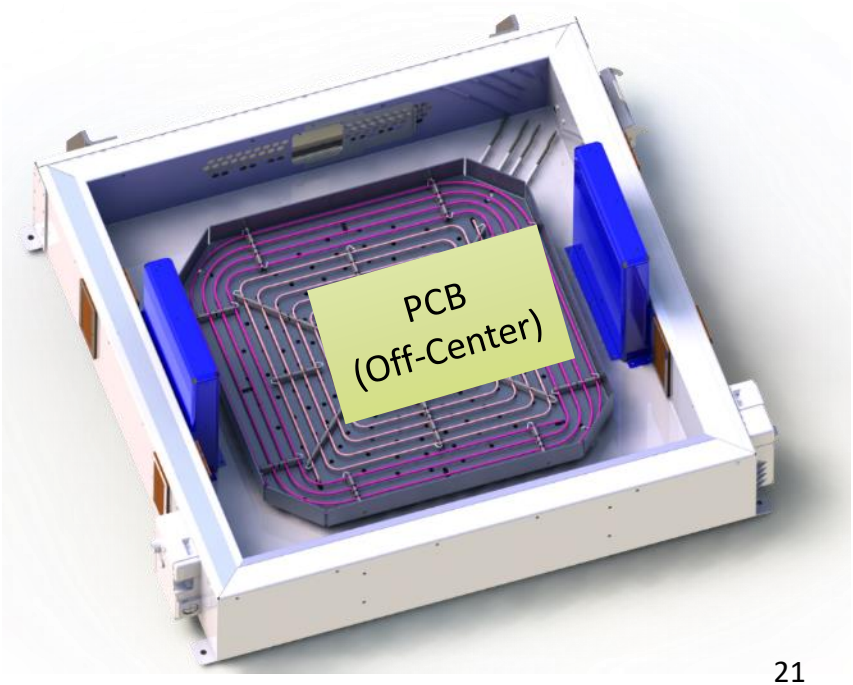
- PCBs in multi-zone reflow ovens receive increased heating on the leading of the PCB prior to the following edge
  - Temperature differentials will vary based on oven, number of zones, profiles, and belt speed
  - This effect is emulated in the case study



Concepts – Creating Lateral Non-uniformity

- Thermal warpage metrology tools are generally designed around even temperature uniformity, but in some cases intentional temperature bias can be created
  - In this case study temperature bias is created by offsetting the PCB from the center of a multi-zone oven, where inner and outer zones can be given variable power percentages





Concepts – Heating Rates vs. Temperature Uniformity

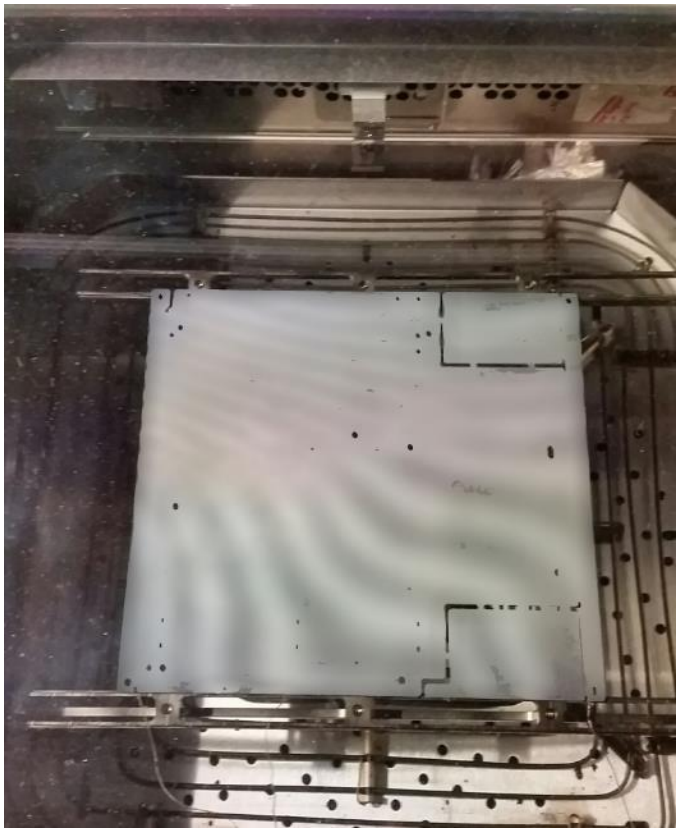
- From a mechanical perspective surface warpage is caused by CTE mismatch of materials and is independent of heating rates
  - Heating rate can play a role in warpage if increased exposure time at elevated temperatures affects the materials with the PCB
  - Experimentally it can be difficult to separate the effects or heating rate and temperature uniformity due to conduction through the PCB
  - In production a change in heating rate or range may be necessary as it relates to the chemistry of solder ball attachment
  - A temperature profile change may also play a role in warpage
  - Efforts were made to keep heating rate a constant in this case study

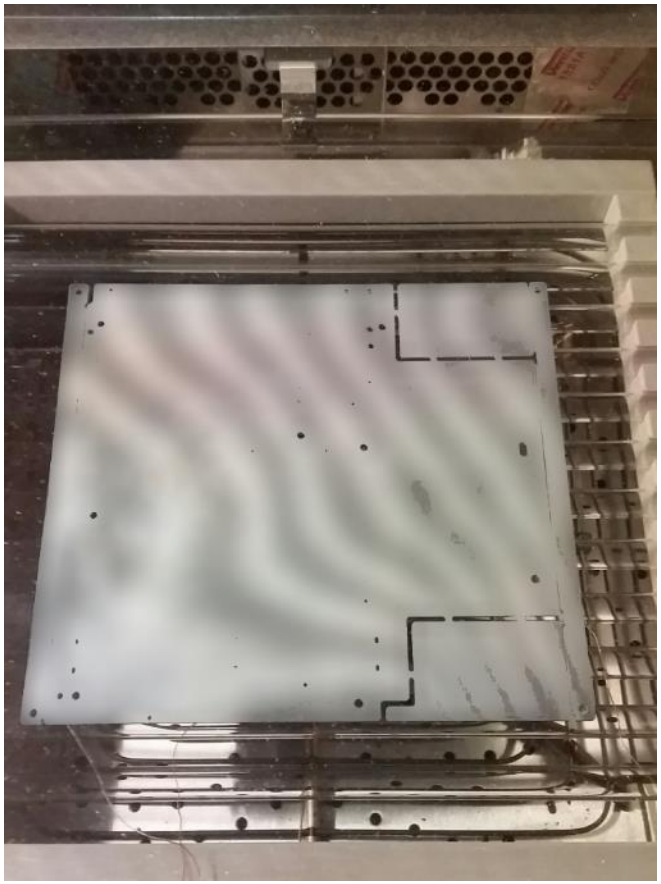
Case Study Test Plan

- Controls
  - Profile: 250°C max Pb free reflow with 9 acquisitions over temp.
  - Reflow cycles: Data from the 1st PCB reflow is excluded
  - Sample Prep: Prebake 12-24 hours at 125°C, light coat of white paint
  - Top/Bottom Temp. Uniformity: All efforts were made to maintain even top/bottom sample temperature uniformity (top heaters in use)
  - Sample: 255x237x1.6mm PCB, 1 form factor, 2 suppliers, 2 samples per supplier
  - Thermocouples: K-type, 36”, 36 gauge. Attached to the bottom middle, left and right of the PCB
  - Measurement Technique: Shadow moiré with 100LPI grating
  - Lighting and Iris
  - Working Distance: 150 mils with 400 mil lower while heating

Case Study Test Plan

- Independent Variables
  - Sample Support Method: Edges or Area Support (15mm quartz bulbs)





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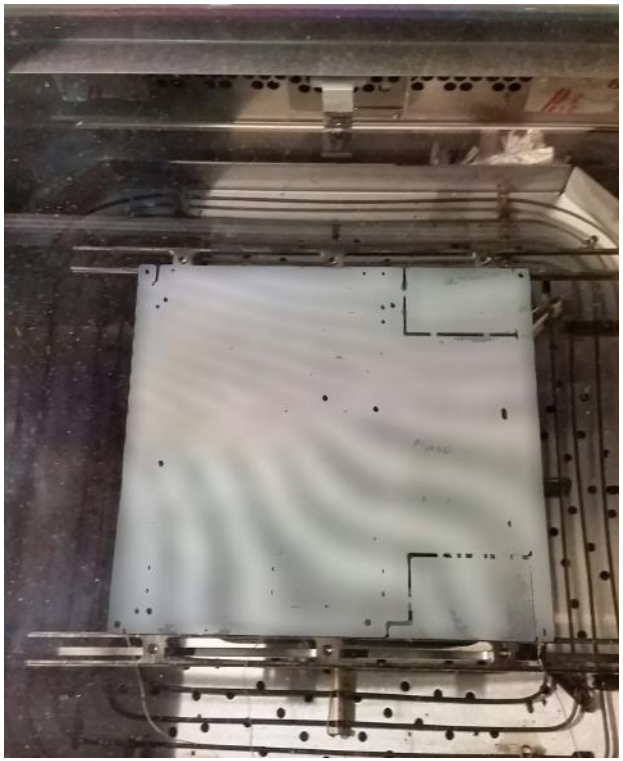
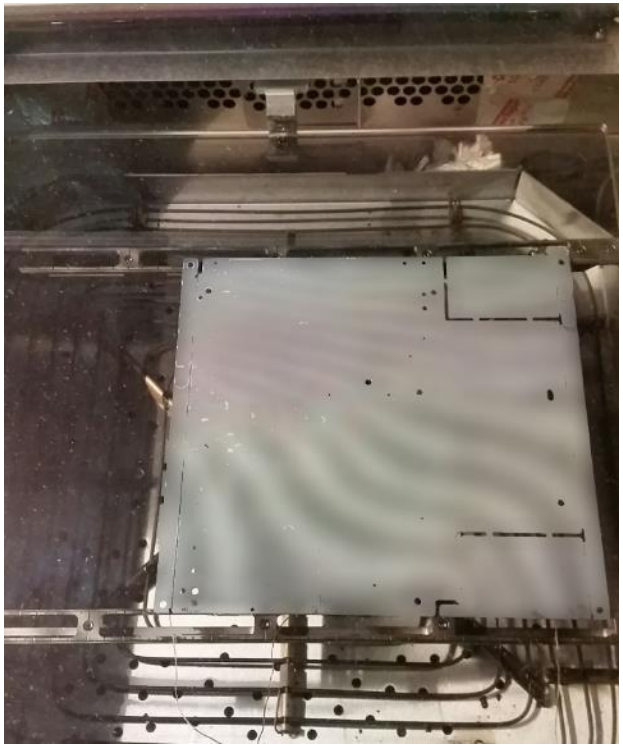
Case Study Test Plan

- Independent Variables
  - Temperature Uniformity: Even heating, ≈25°C temp. differential right side hot, ≈25°C temp. differential left side hot





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Case Study Test Plan

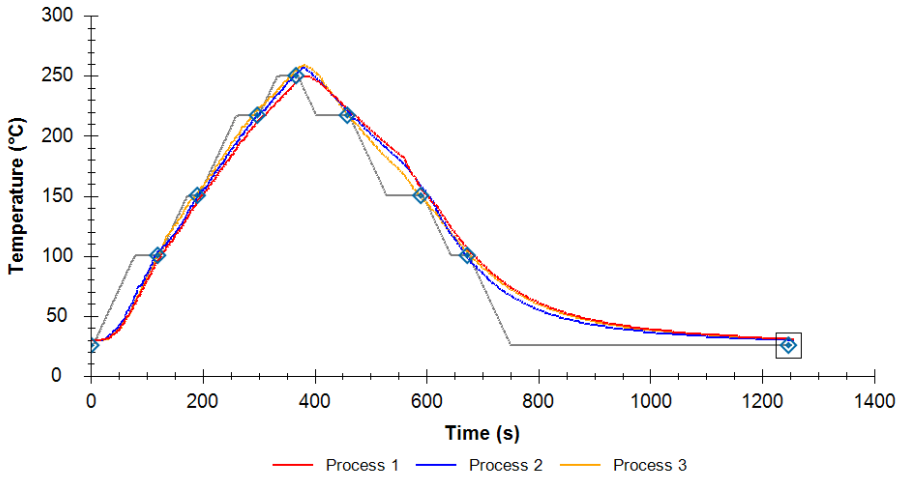
- Dependent Variables
  - PCB Global
    - JEDEC Full Field Signed Warpage (JFFSW)
    - Bow
    - Twist
  - PCB Locals
    - JEDEC Full Field Signed Warpage (JFFSW) of…
      - 30x30mm BGA Attach
      - 32x32mm BGA Attach
      - 35x35mm Socket Attach

Case Study Test Plan

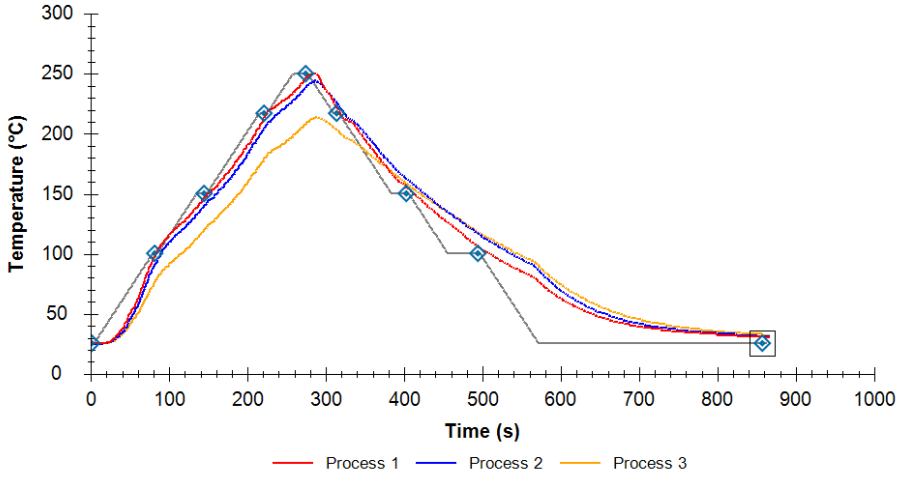
- Hypothesis
  - Area support will reduce global JFFSW, bow and twist
  - Area support will have minimal effect on local JFFSW
  - A lack of temperature uniformity will cause shape change in the PCB
    - Sample warpage should be considered on a relative basis

Case Study Results – Thermal Profiles

≈ Even



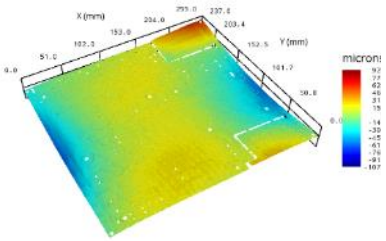
≈ 25°C Differential



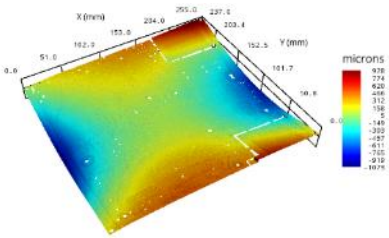
Case Study Results

- Typical Warpage Example – Global

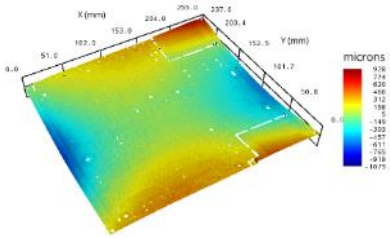
30C



98C



148C



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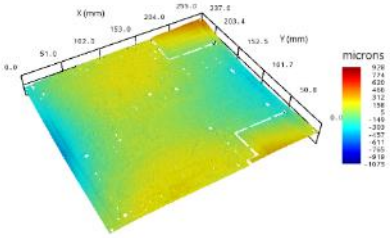
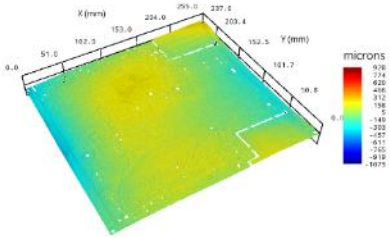
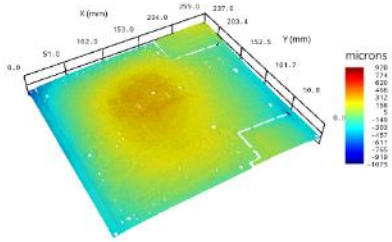


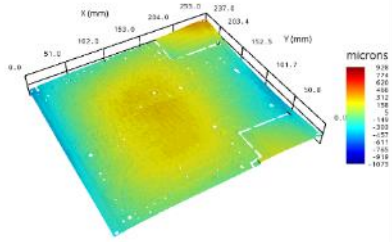
247C



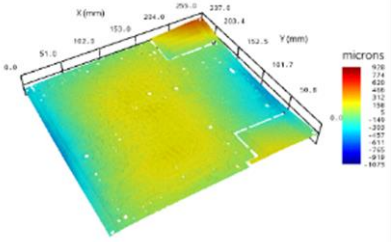
219C



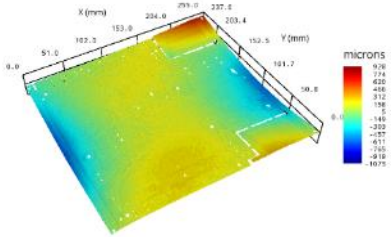
152C



103C



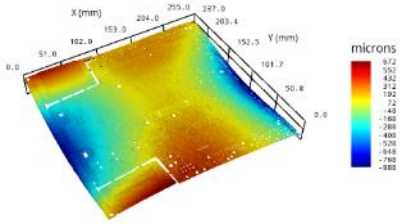
30C



Case Study Results

- Non Uniformity Example – Global

30C



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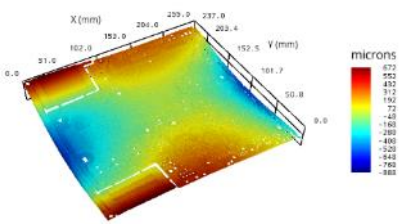
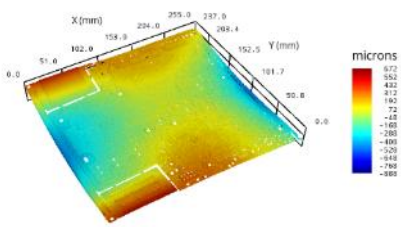
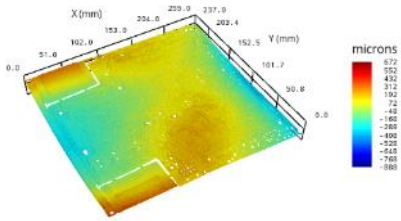


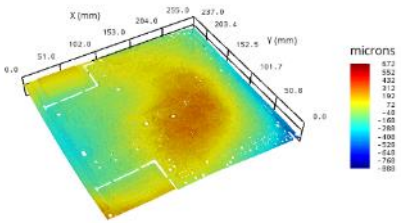
148C



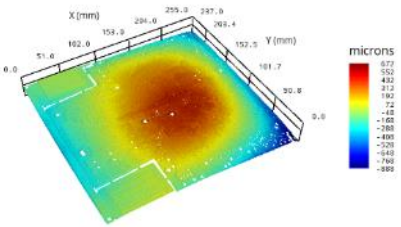
215C



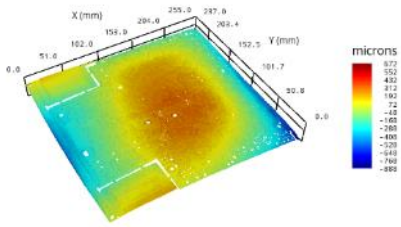
247C



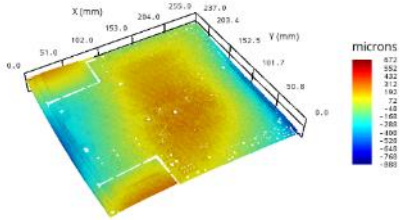
219C



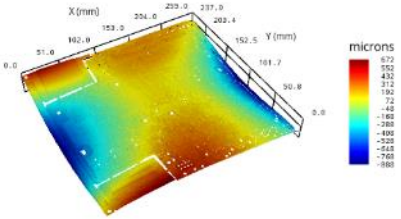
152C



103C

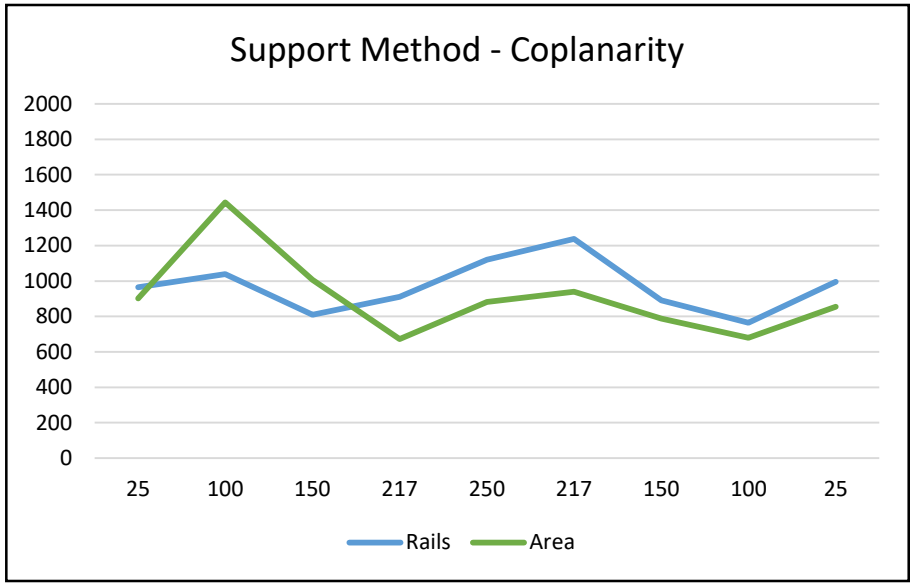


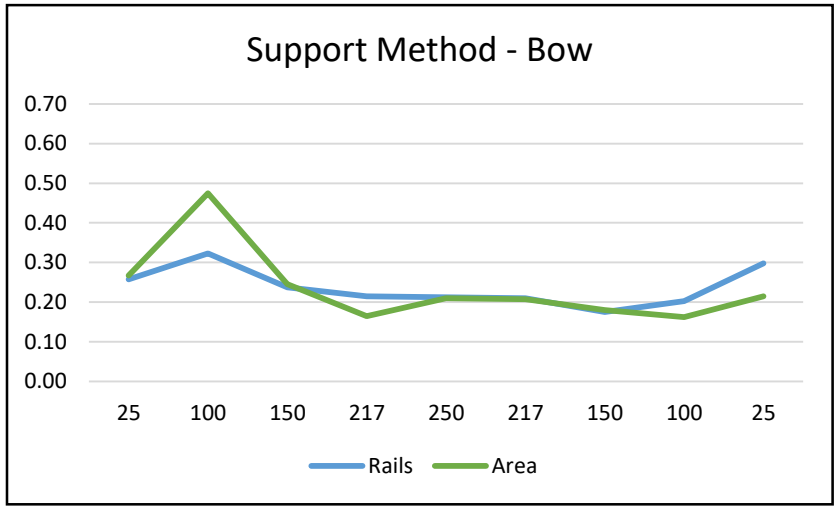
30C

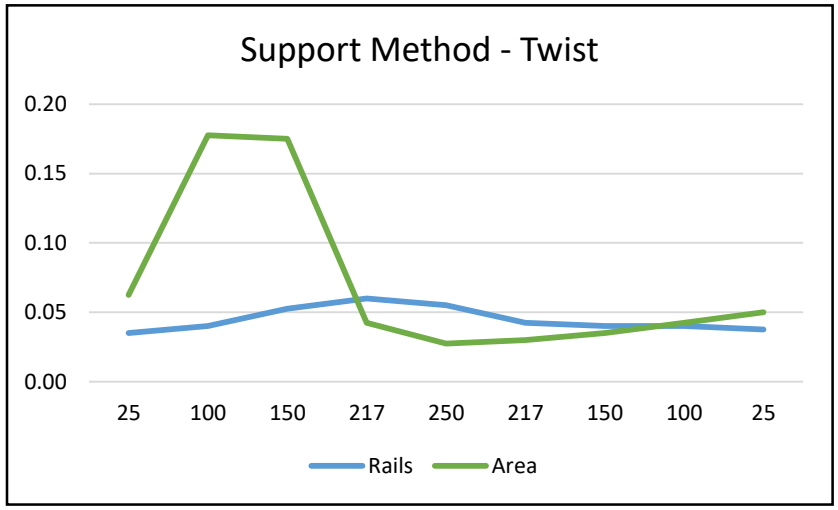


Case Study Results

- Gauge Results – Global – Sample Support Method

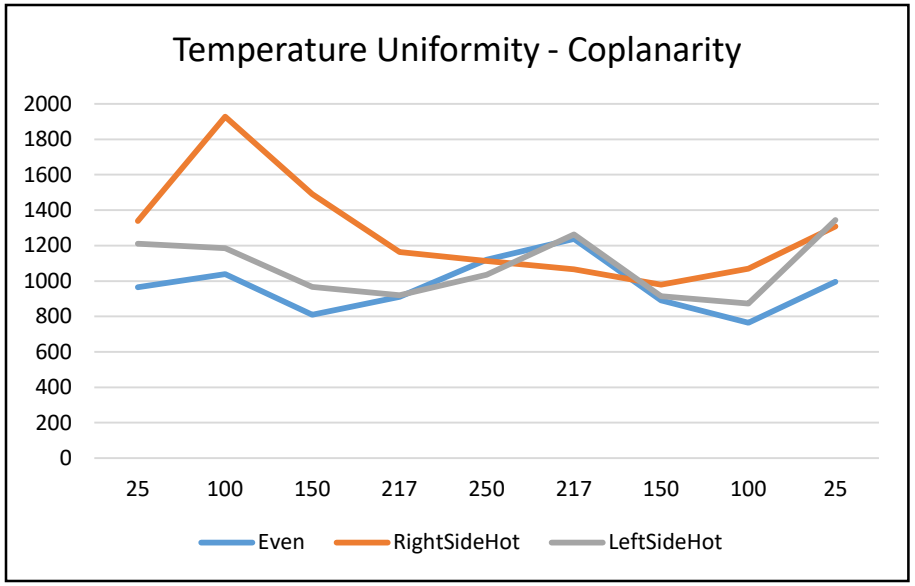


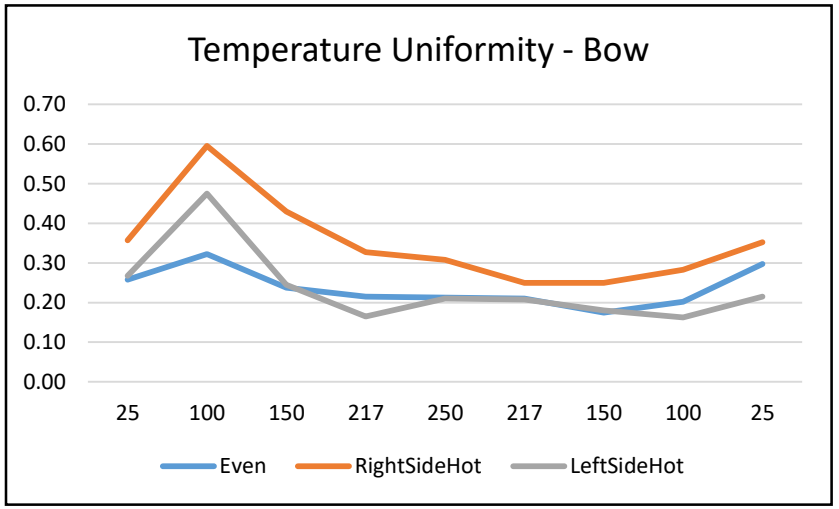


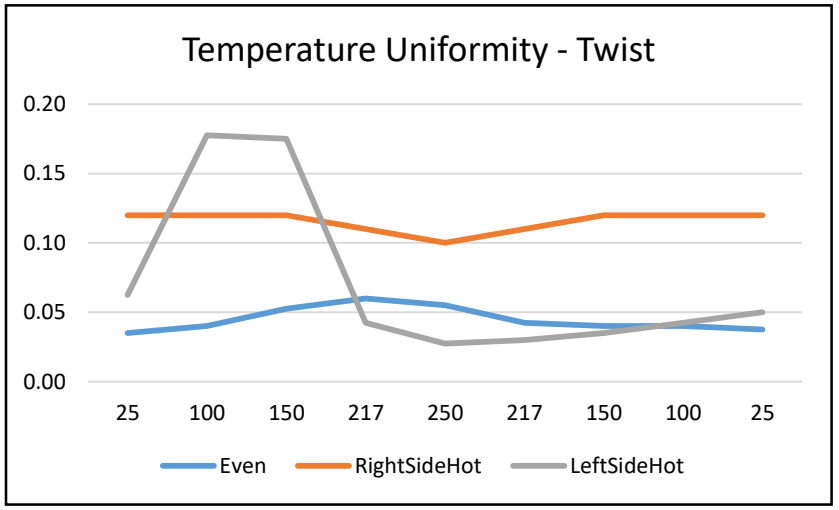


Case Study Results

- Gauge Results – Global – Temperature Uniformity

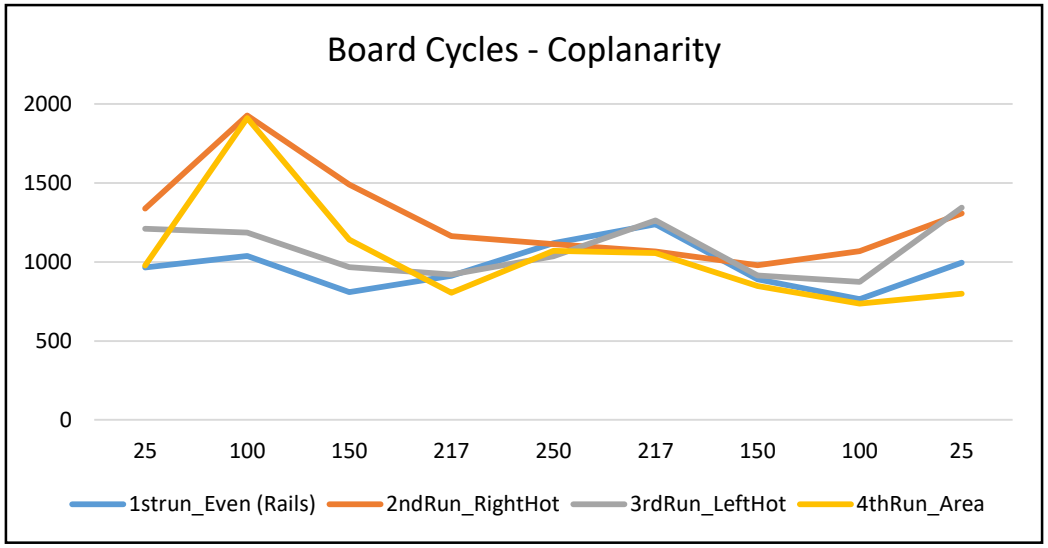






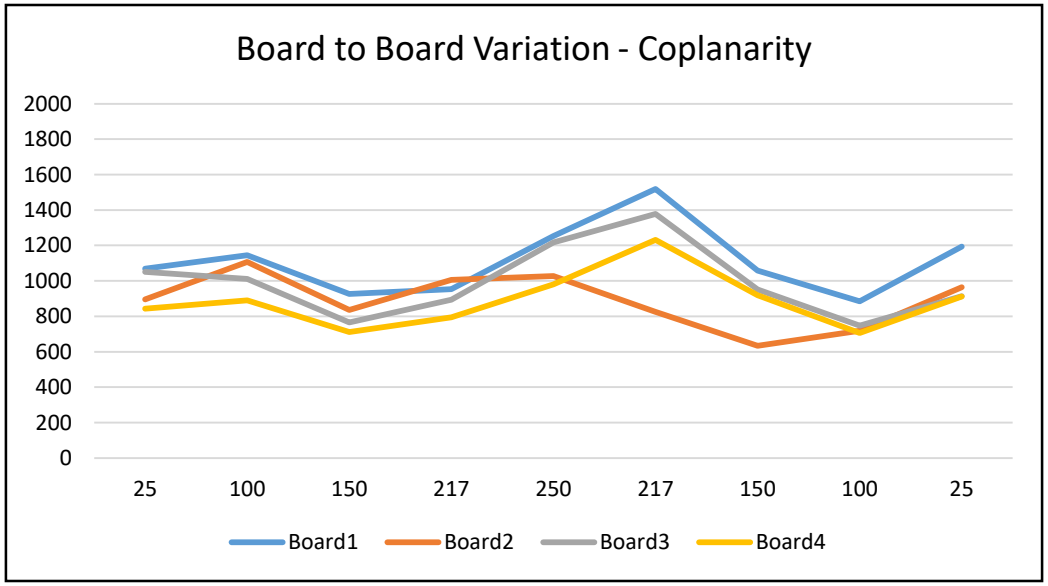
Case Study Results

- Control Issue – Board Cycles
  - While 1st run reflow profiles were thrown out, it appears that for this PCB there was a general increase of coplanarity through various thermal cycles
  - The choice of 250°C as a max temperature for the PCBs may have been too high
  - Some signs of delamination was seen
  - Excluded outlier of a single board from Area support



Case Study Results

- Gauge Results – Board to Board Variation
  - Results from uniform heating with edge support

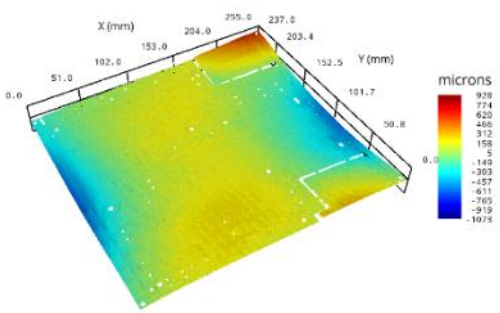


Case Study Results

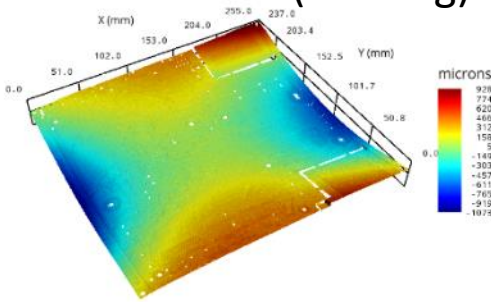
- Relative Warpage
  - Measure the change in shape of the surface rather than the absolute shape

Absolute Shape

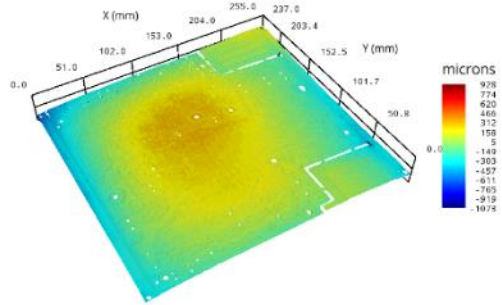
25C



100C (Heating)

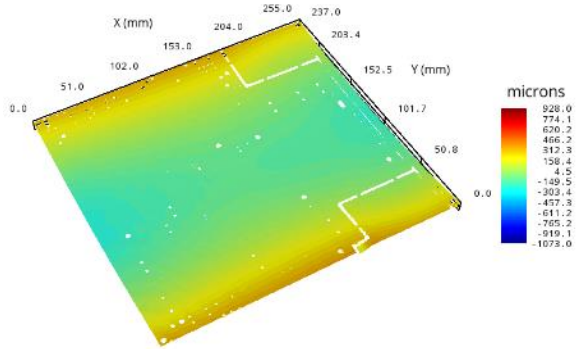


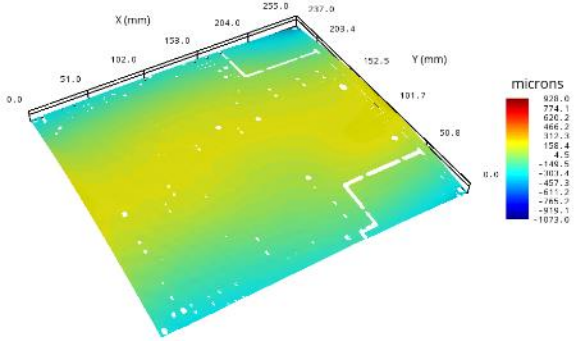
220C (Cooling)



Relative Shape Change

100C - 25C

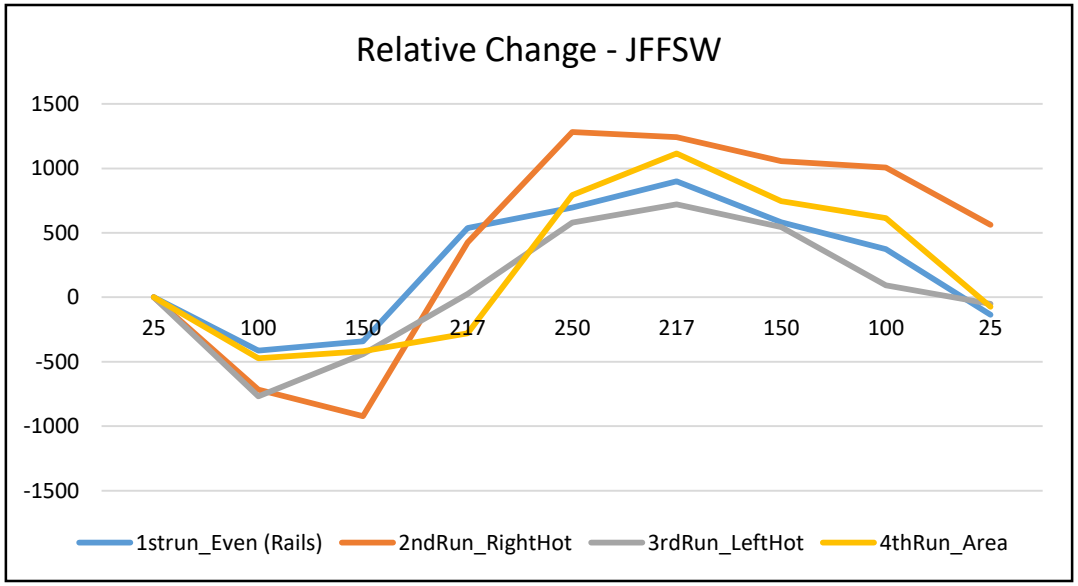




220C - 25C

Case Study Results

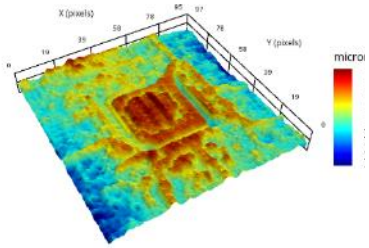
- Relative Warpage
  - Measure the change in shape of the surface rather than the absolute shape
  - Change in shape more consistent with direction of warpage
    - Signed Warpage can be used (JFFSW)



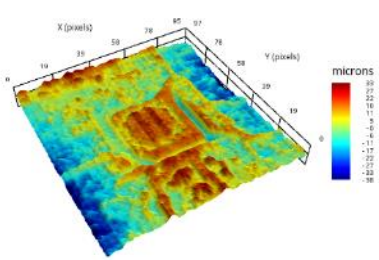
Case Study Results

- Typical Warpage Example – Local 1

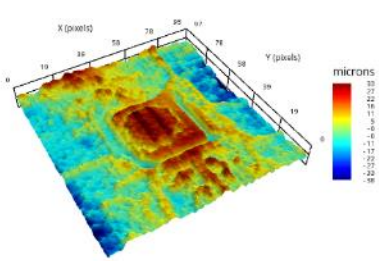
26C



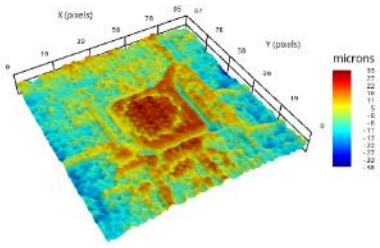
99C



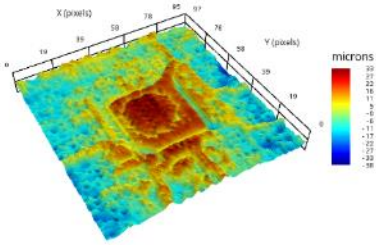
147C



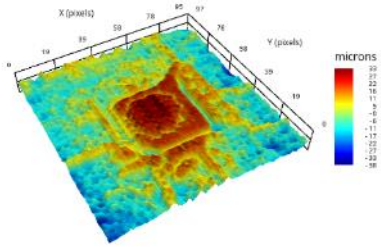
214C



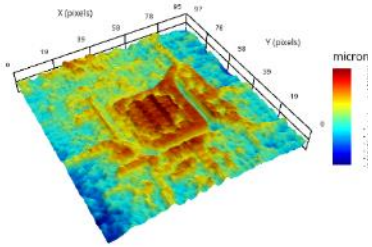
247C



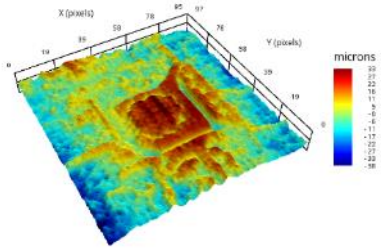
219C



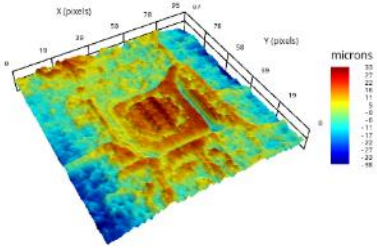
153C



103C



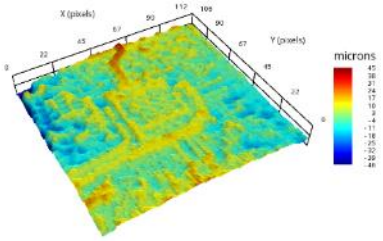
30C



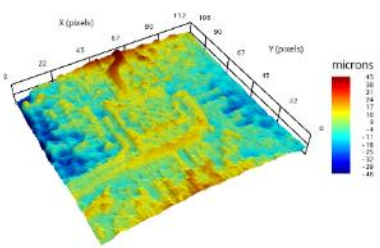
Case Study Results

- Typical Warpage Example – Local 2

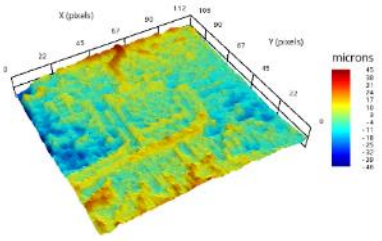
26C



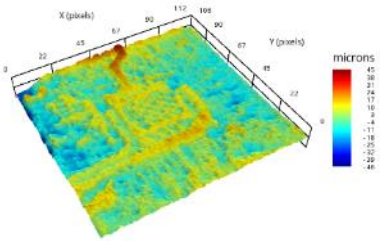
99C



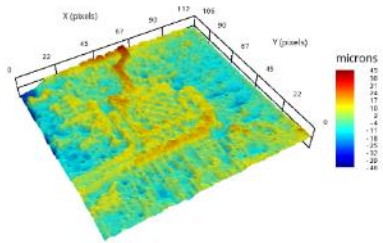
147C



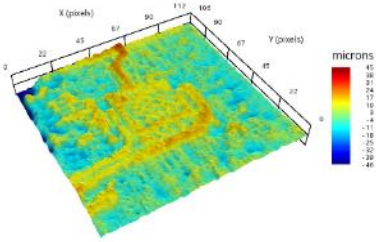
214C



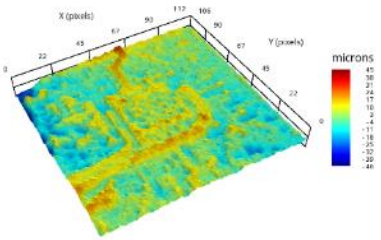
247C



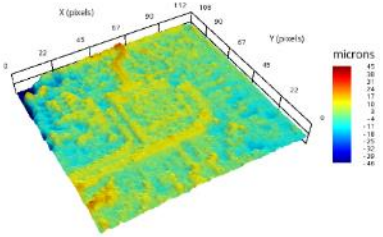
219C



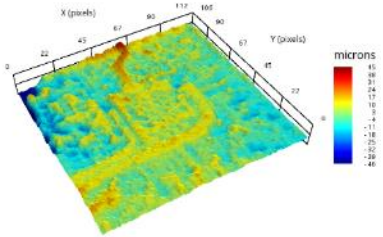
153C



103C



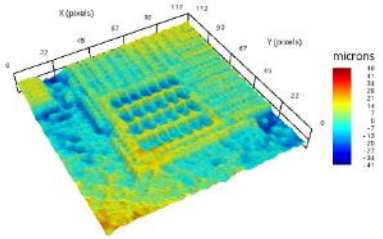
30C



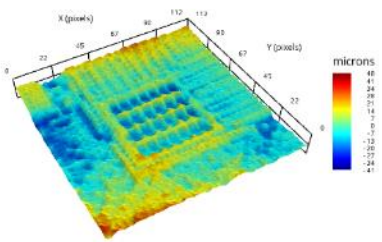
Case Study Results

- Typical Warpage Example – Local 3

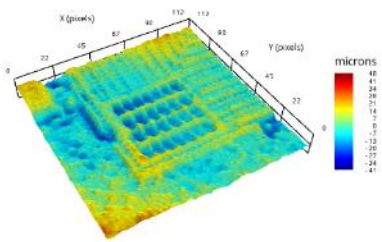
26C



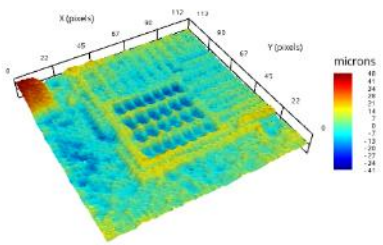
99C



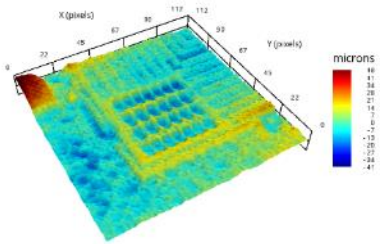
147C



214C



247C



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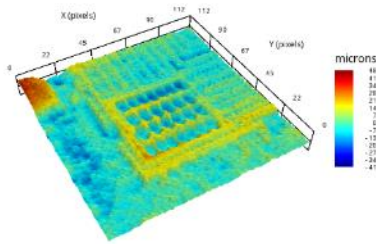
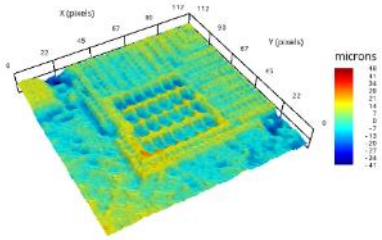
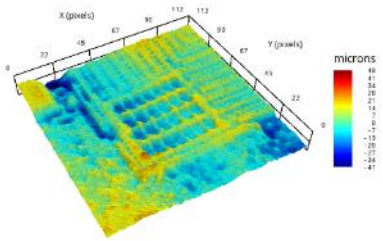


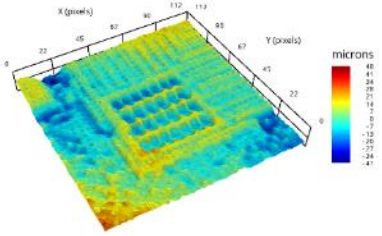
153C



103C

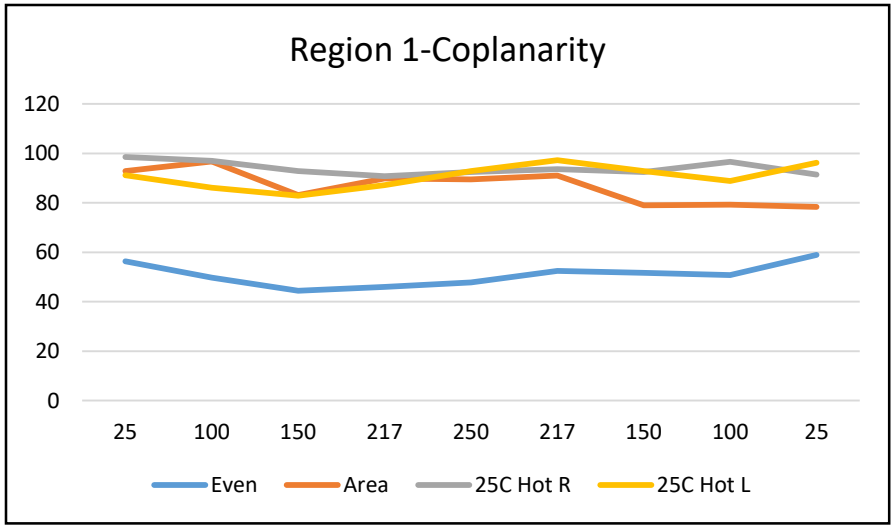


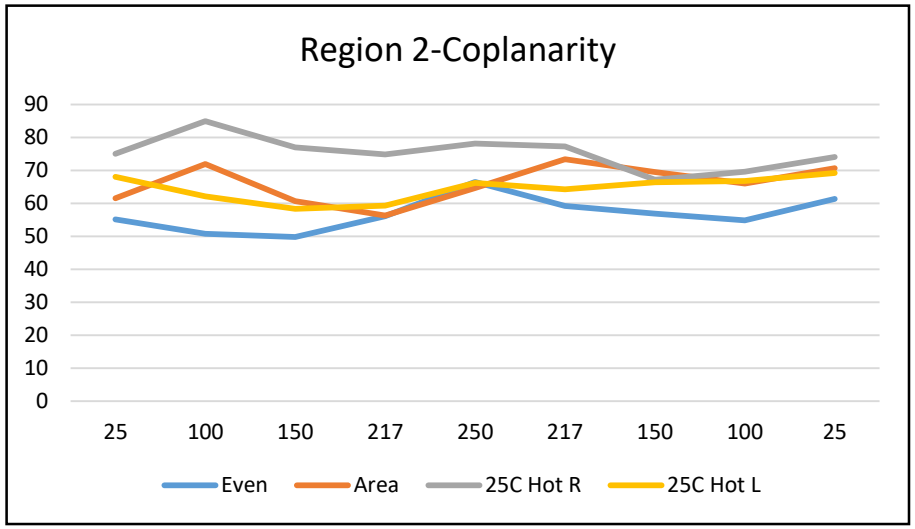
30C

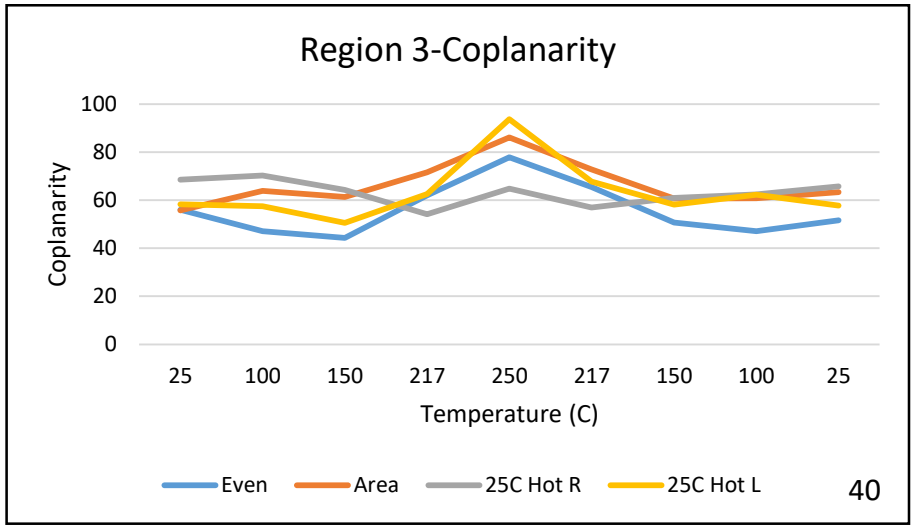


Case Study Results

- Gauge Results – Local – Sample Support and Temperature Uniformity

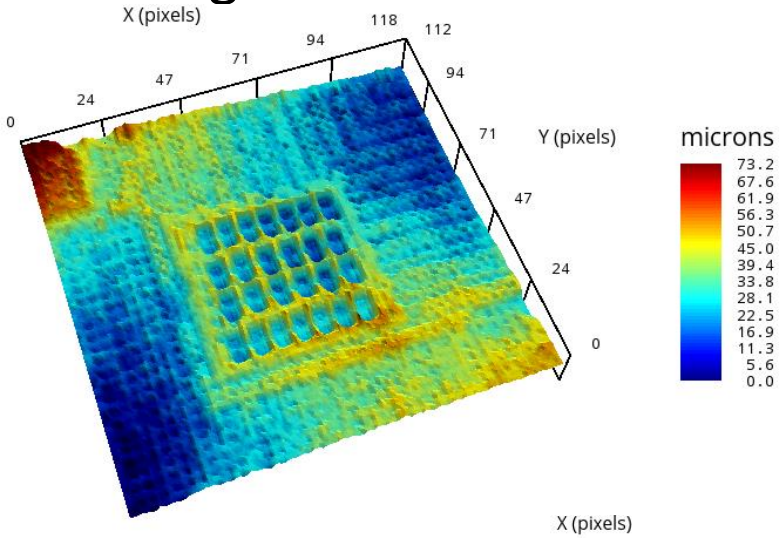




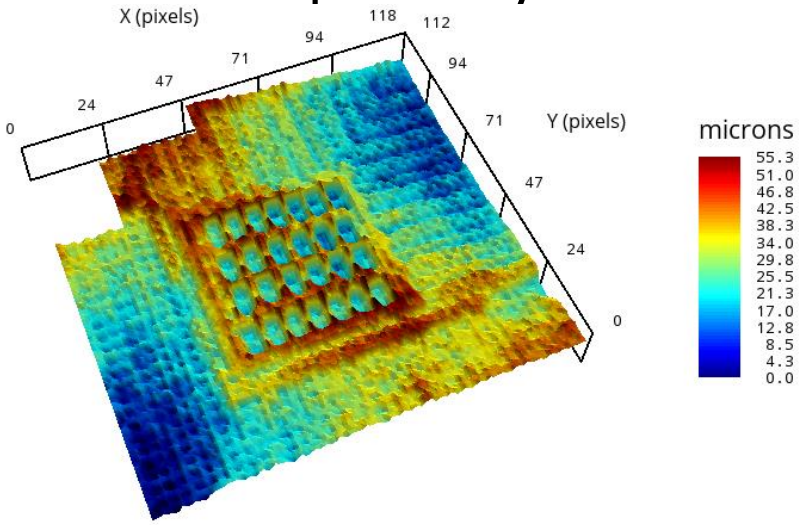


Case Study Results

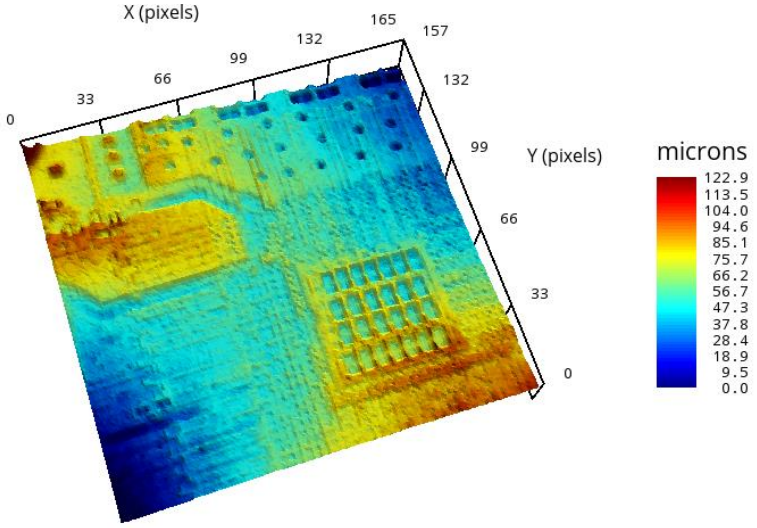
- Gauge Results – Local – Board Features Affect Coplanarity



Coplanarity = 73.2 microns



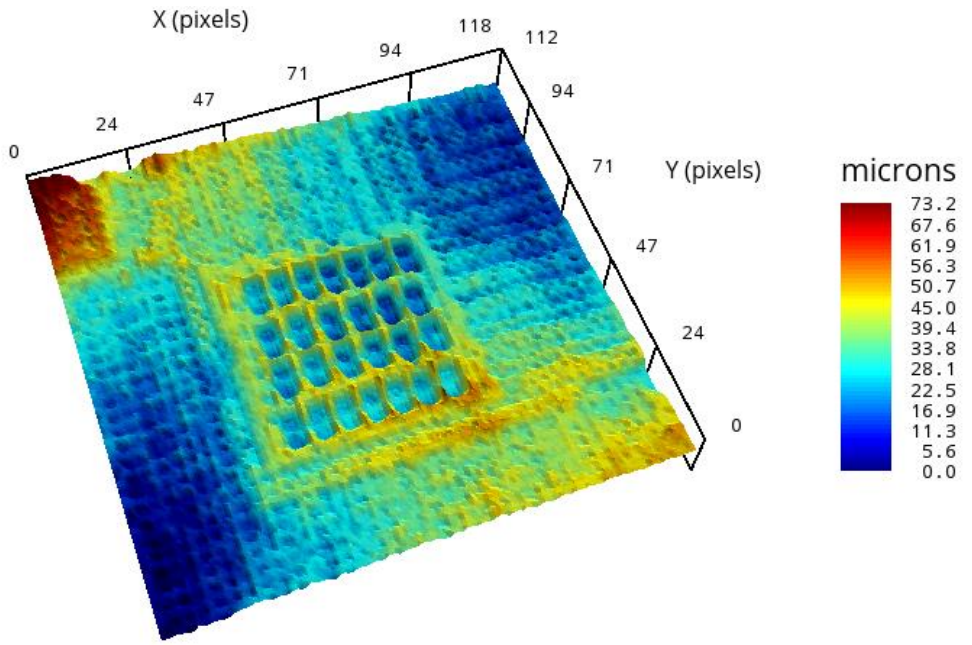
Coplanarity = 55.3 microns



Coplanarity = 122.9 microns

Case Study Results

- Gauge Results – Local – Gauges Choices
- Bow = -0.07%
- Twist = 0.10%
- JFFSW = 73.2 microns
  - Signal Strength = 4.16%
  - Shape Name - Upward Twist
- Radius of Curvature = 72.7 meters



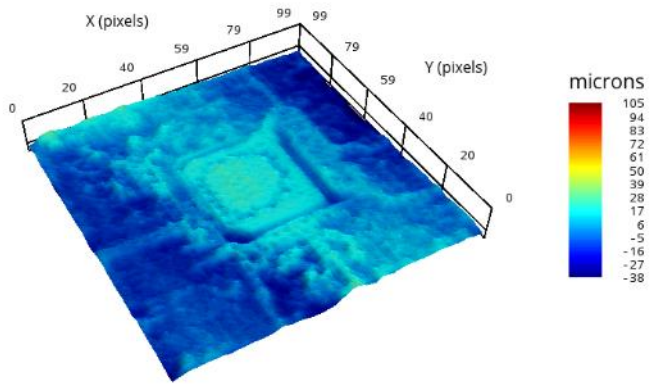
Coplanarity = 73.2 microns

Case Study Results

- Gauge Results – Local – Delamination
  - Board Delamination around Region 1 caused outlier for warpage data

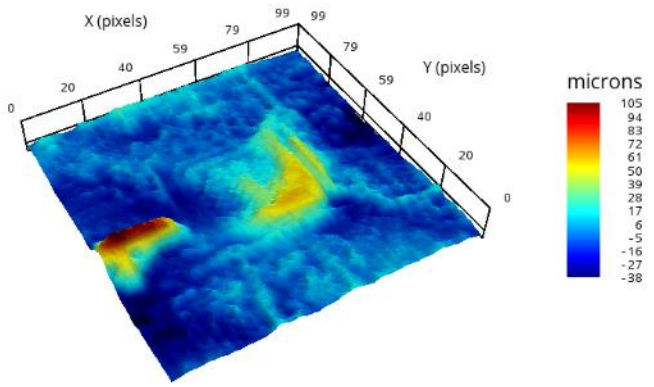
Before Delamination

25C



After Delamination

26C



Lessons Learned

- Gauge Results often don’t fully describe surface shape for PCBs
- Quantitative results were inconclusive
- Differences in warpage with respect to temperature uniformity can be resolved from qualitative analysis
- Non uniform heating can lead to different shape change
- Support method played no tangible role in surface warpage for boards at the tested thickness
- Local area warpage is largely influenced by PCB surface features
- Sample to sample variation at room temperature prevalent
- Multiple reflow cycles on test PCBs played a large role in study

Potential Future Work

- Use higher quantity of PCBs and 1st reflow behavior in future studies
  - Will need enough to remove sample to sample variation
- Run tests with thinner PCBs to show effects of sample support method on warpage
- Follow through with iNEMI and MTC studies in progress
- Move towards local area PCB warpage standard based on surface mount attach pitch and feature height
  - Standard may be most effective if not deciding pass/fail on surface coplanarity, but rather another gauge or combination of gauges

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YOUR FEEDBACK IS IMPORTANT! DON'T FORGET TO COMPLETE YOUR SPEAKER EVALUATION.

PLEASE REMEMBER TO RETURN THE EVALUATION FORMS TO THE REGISTRATION DESK OR TO THE DROP BOX IN THE LOBBY.

THANK YOU,

PCB WEST SHOW MANAGEMENT