Shadow Moiré Enters Production

By Kathleen McCray

A little more than a year ago, this column outlined a new technique for characterizing board and device warpage with respect to temperature.[1,2] At that time, the instrumentation was designed for use in the laboratory. This column describes the unique developments that have been accomplished to bring shadow moiré technique to the production floor.

While shadow moiré is a naturally occurring phenomenon and the technique has been realized for many years, the use in this system is quite genius. Briefly, the shadow moiré method is an optical method that measures the topography of the surface of a solid object. Here a reference grating, which is comprised of transparent and opaque equal spaces on a flat glass substrate, is positioned above the surface of the sample. When the white light illuminates the grating, it projects the shadow of the grating onto the surface of the sample. The shadow of the grating is distorted due to the warpage of the sample. Moiré fringes are then generated by the geometric interference of the shadow grating and the real reference grating. Fringes are commonly viewed at an angle normal to the surface of the grating. Fringes are lines composed by the points along the sample having equal distance between the grating and the surface of the sample.

When the surface of the sample deviates from a flat plane or is not parallel to the grating, the fringe density is high; otherwise, the fringes are sparse. From the governing equation of shadow moiré,

$$w = Np/\tan \alpha + \tan \beta$$

The displacement that each fringe represents is equal to the pitch (p) of the grating if the illumination angle α is 45° and the observation angle β is 0°; w is the out-of-plane displacement and N is the fringe order.

Phase-Stepping Technique

Now, as has been noted, the shadow moiré technique is not new; however, the software that equips the instrument is the key to the system. In fact, the software component termed "phase-stepping" is what enables the system to successfully characterize the warpage of a particular device with a sensitivity of better than ±0.1 mils (±2.5 µm). A description of the phase-stepping routine follows.

Fringes produced by shadow moiré are equal value lines, representative of the distance between the sample surface and the grating — i.e., each point in a given fringe is in the same plane. When the grating is translated in the Z-axis closer to or further from the sample surface, a given fringe will move toward a lower order or higher order, respectively. Phase-stepping technique generates multiple fringe patterns by shifting the grating a fraction of the distance p to obtain fine fractional fringe orders. The sensitivity of the fringe pattern image analysis is increased significantly by this technique. One important advantage of phase-stepping is that the direction of the warpage is automatically determined due to the nature of the fringe shifting.

The problems that can be addressed by this novel technique are far reaching. With the availability of equipment that can characterize surface topography of substrates prior to performing value-added processes, many failure mechanisms historically unknown can be identified.

Production-Line Integration

While the original system was designed for the laboratory, and is still currently available, the new system is able to inspect printed wiring boards (PWBs) and chip-carriers in the production line. Most impressively, this system can evaluate an entire JEDEC tray and provide information on the magnitude, location and type of warpage of each part in the tray (Figure 1). Additionally, standard pass/fail criteria is already programmed into the system (Figure 2). These criteria are based on current-day specifications already in use by suppliers and assemblers.

The system operates at room temperature and inspects substrates for coplanarity, bow, twist and waviness. Moreover, like its laboratory counterpart, this system is a full-field measurement technique. In other words, data is collected simultaneously across the entire surface of the sample under evaluation. This provides substantial amounts of quantitative data for analyses. For example, in a tray of 40-mm chip carriers, there will be up to 3,500

Key Points of Application in Production:

PWB fabrication	Bow and twist check prior to shipping; image transfer analysis.
Device packaging	Coplanarity of chip carriers prior to die placement; stiffener/heat sink flatness inspection.
Surface-mount lines	Inspect coplanarity, bow and twist of key component sites on PWBs at front of flow line; board/component site warpage between multiple reflows.

HDI Terms and Abbreviations

AOI ..... automated optical inspection
ATE ..... automatic test equipment
BGA ..... ball grid array
CAD ..... computer-aided design
CGA ..... column grid array
CM ..... contract manufacturer
COB ..... chip on board
COFO ..... closed loop force control
CSP ..... chip-scale package
CTE ..... coefficient of thermal expansion (also TCE)
DCA ..... direct chip attach
DSP ..... digital signal processor
ECU ..... electrical control unit
EFO ..... electronic flame-off
EMI ..... electromagnetic interference
EMS ..... electronic manufacturing services
etCSP ..... extremely thin chip-scale package
FABD ..... free air ball diameter
FCB ..... flip chip bump
FEM ..... finite element model
FOC ..... flex on cap
FPLD ..... field programmable logic device
HDI ..... high-density interconnect
HTLM ..... high temperature low modulus
I/O ..... input/output
IC ..... integrated circuit
IMAPS ..... International Microelectronics and Packaging Society
KGD ..... known good die
MCM-D ..... deposition multichip module
MCP ..... multichip package
MEMS ..... microelectromechanical systems
MFC ..... mass flow calibration
MRAM ..... magnetic random access memory
MV ..... microvia
OBC ..... optical bond centering
OEM ..... original equipment manufacturer
PBGA ..... plastic ball grid array
PDA ..... personal digital assistant
PWB ..... printed wiring board
QFP ..... quad flat pack
RFIC ..... radio frequency integrated circuit
RH ..... relative humidity
S-CSP ..... stacked chip-scale package
SEM ..... scanning electron microscope
SF ..... shear force
SIP ..... system in package
SOC ..... system on a chip
SRAM ..... static random access memory
TAB ..... tape automated bonding
TBGA ..... tape ball grid array
T_g ..... glass transition temperature
TSOP ..... thin small-outline package
UFP ..... ultrafine pitch
UV ..... ultraviolet
VFM ..... variable frequency microwave
WL-CSP ..... wafer-level chip-scale package
WLP ..... wafer-level packaging
ZIF ..... zero insertion force

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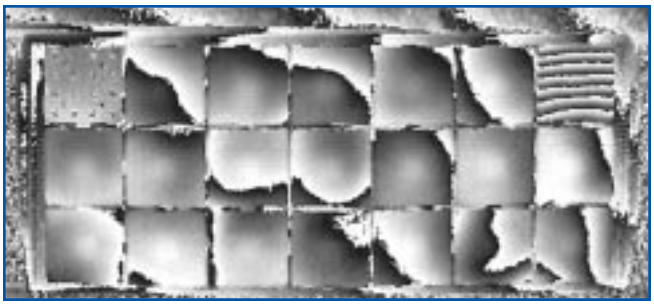

FIGURE 1: Full-field data set (i.e., fringe pattern image) of a JEDEC tray full of 40-mm substrates.

data points per device for analysis. With this amount of data, the user now has an incredibly powerful means to improve inspection parameters. Historically, as few as two to three data points have been used for pass/fail decision. This led to the misidentification of devices that were both good and bad.

With the ability to duplicate just about all existing flatness checks — i.e., two-point analysis, five-point analysis, coplanarity, etc. — the system can be implemented into existing lines at once and provide immediate increases in throughput. Users can then work to identify advanced warpage characteristics and how they impact production defects. Defect correlation studies can then be used to set new test parameters for the shadow moiré-based system. ■

References

1. Kathleen McCray, "New Techniques Rise to the Occasion," *HDI*, June 1999, p 18.
2. Kathleen McCray, "Analytical Real-Time Techniques Rise to the Occasion: An Illustration," *HDI*, July 1999, p 16.

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Kathleen McCray is president of Diversified Technologies Resources Inc., (719) 548-8356, e-mail: kmccray@email.msn.com.

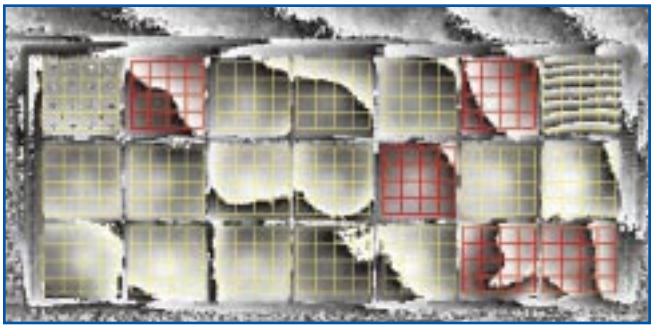

FIGURE 2: Individual devices are analyzed for coplanarity and a pass/fail reading is provided. Red areas indicate "failed" parts on a 6-mil (150-µm) flatness specification.