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ADVANCED WARPAGE CHARACTERIZATION: *LOCATION* AND *TYPE* OF DISPLACEMENT CAN BE EQUALLY AS IMPORTANT AS MAGNITUDE

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ABSTRACT

Warpage characterization of components and substrates began to gain in importance with the development of area array devices – most notably the BGA. Today, packagers and assemblers are faced with a multiplying amount of packaging formats and advanced substrates that demand tight mechanical tolerances. While designs have advanced tremendously, the extent to which we routinely characterize warpage has progressed limitedly at best.

In-process warpage evaluation of devices and substrates is proving to have significant value not just in the design and reliability phases, but also in the roll of production diagnostics and production yield improvement. In-process warpage analysis is being used in pre-production applications to qualify each component and substrate design to be assembled on a flow-line (package assembly and board assembly).

By fully characterizing device and substrate behavior prior to production, assemblers can significantly reduce in-line defects related to adverse mechanical behaviors. Two cases where pre-production investigations resulted in significant processing yield improvements are examined. Data presented shows that characterizing the type and characterizing the location of warpage can be as critical as characterizing the magnitude of warpage.

Advanced warpage characterization is hypothesized to be valuable to solder joint reliability investigation. Interconnect analysis, together with reliability analysis, will be two critical areas of mechanical property focus with the introduction of lead-free solders and bromine-free laminates.

It is concluded that advanced characterization of warpage can be an important means for reducing interconnect defects. Fewer soldering defects result in fewer units requiring rework – one of the single highest cost elements of assembly and manufacture. Advanced characterization of warpage by evaluating location and type of warpage in addition to magnitude can further enhance defect-free manufacturing initiatives.

Key words: warpage, defects, rework, thermomechanical behavior, characterization.

BACKGROUND

Warpage of printed circuit boards and components can cause significant production and reliability problems. Symptoms of adverse warpage include damaged and misregistered components, solder paste bridging and opens, cracked solder joints, and production line jams. Thermally induced warpage is most prevalent during high temperature manufacturing processes, such as reflow soldering. As substrate designs strive to incorporate finer lines, higher component densities and thinner cross-sections, the relative impact of warped substrates and components is increased.

Traditional means for measuring warpage have been limited to pre-process and post-process inspections. The ability to evaluate in-process warpage was not possible until recently. In 1989 a group of industrial sponsors, including AT&T, DEC, Ford Electronics, IBM, US Army Missile Command, and Motorola, initiated a research project at the Advanced Electronic Packaging Lab (AEPL) of the Georgia Institute of Technology, Atlanta, Georgia USA. The research, led by Dr. I. Charles Ume, resulted in a novel approach to measuring substrate warpage with respect to temperature in real-time [1,2].

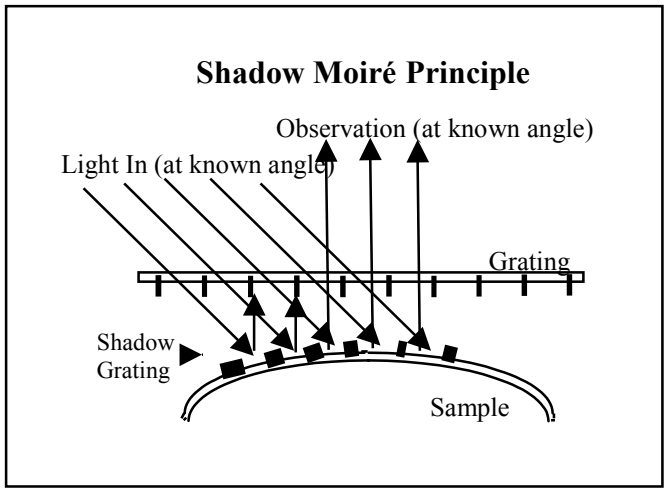
Originally applied to larger area substrates, primarily PCBs, the technology was used to evaluate thermomechanical behavior on a global (i.e. whole board) basis. With the introduction of advanced packaging systems (the BGA especially) to mainstream manufacturing, a second order of warpage concerns for electronic packages and assemblies was created. Component packages and substrates also have design specific warpage behaviors induced by temperature. The ability to evaluate warpage magnitude of advanced package designs at temperature was important for both reliability and interconnect reasons.

The thermomechanical deformation of a BGA during processing is of significant concern to engineers and designers due to its potential to adversely affect the manufacture and robustness of the assembly. Mismatched CTE values of package materials can cause significant stresses potentially resulting in package delamination or even die cracking. Package construction variables and material properties can create mechanical deformations of magnitude that adversely affect solder ball interconnect with the component's seating plane on the PWB.

Shadow Moiré Technique

Shadow moiré technique measures the topography of the surface of a solid object, *i.e.,* its deviation from a planar surface [1]. Figure 1 is a schematic of the shadow moiré principle and its components. A reference grating, which is comprised of transparent and opaque equal spaces on a flat glass substrate, is positioned above the surface of the sample. When white light illuminates the grating, it projects the shadow of this grating onto the surface of the sample under observation. The shadow of the fixed reference grating is distorted due to the warpage of the sample surface. When observed from a different angle (in this case normal to the surface of the sample), moiré fringes are generated by the geometric interference of the shadow grating and the real reference grating. Fringes are lines composed by the points along the sample having equal distance between the reference grating and the surface of the sample.

Figure 1. Shadow moiré principle shows how a geometric interference pattern in created by the observation of the shadow grating through the fixed reference grating.



When the surface of the sample deviates from a flat plane or is not parallel to the grating, fringes are visible. In the event that a sample is perfectly flat and positioned parallel to the reference grating, no fringes are present. From the governing equation of shadow moiré,

$$w = \frac{Np}{\tan\alpha + \tan\beta}. \qquad (1)$$

Fringes are readily converted to quantitative information that characterizes displacement. Fringe value (measurement resolution) is equal to the pitch (p) of the grating if the illumination angle α is 45° and the observation angle β is 0° as it is presented in Figure 1. In eq.(1), w is the out-of-plane displacement and N is the fringe order (i.e. number of fringes). Traditionally, the value of the out-of-plane displacement at an interested point in the field is determined by counting the fringe order at that point from a selected reference point. Interpolation is applied because the point does not always fall onto a fringe center. The accuracy of fringe counting analysis is about 20 percent. Dependent upon grating resolution, the highest fringe sensitivity that shadow moiré delivers is approximately 25 μm [3].

Phase-Stepping Analysis

The fringes of shadow moiré are equal value lines of the distance between the sample surface and the grating. When the grating is translated (z-axis) closer to or further from the sample surface, a given fringe will move towards a lower order or higher order, respectively. When the grating is translated a distance of p away from the sample, the fringe will shift up one complete fringe. When the grating is translated a distance of fractional p, the fringe will shift a fractional fringe space. Phase-stepping analysis uses multiple fringe patterns that are shifted a known amount to obtain fine fractional fringe orders. The sensitivity of the fringe pattern image analysis is increased significantly by this approach. In addition to increasing the analysis sensitivity to better than 2.5 microns, the direction of the warpage is automatically determined due to the nature of the fringe shifting [3].

Phase-stepping uses all the grayscale information provided by the fringe images. Changes in light intensity for each pixel are correlated to changes in z-axis translation. Since the z-axis translation is a known amount, solving for the light intensity is required. The distribution of light intensity of a fringe pattern image obtained from shadow moiré can be approximated by a sinusoidal function,

$$I = I_0 + A\cos[\varphi(x,y)], \qquad (2)$$

where, I is the light intensity, I_o is the background light, A is the modulation of the fringe and φ is the phase term. The fringe number N is simply equal to $\varphi/2\pi$, therefore, finding out fringe number N is to determine phase term φ in eq. (2).

The phase term φ is determined by taking a number of fringe pattern images ñ shifting the fringe pattern image a certain amount for each acquisition ñ and applying a least squares algorithm to solve for the unknowns of equation (2) [4,5]. A minimum of three images is necessary because there are three unknowns, background light I_0, modulation of the fringes A, and phase φ. It is noted that among the three unknowns, only φ is needed to solve explicitly. Generally, the more images that are taken the less error that is seen [5]. However, in practice, the less images taken, the greater the data acquisition rate and the lower the required storage memory.

Phase-stepping analysis provides the high sensitivity required for small magnitude displacements. When combined with an unwrapping algorithm, phase-stepping

provides a data set that can be readily used by the engineer. Specifically, a matrix of displacement values is created. Each pixel from the CCD image is assigned a z-axis value that characterizes the surface of the sample being evaluated.

MAGNITUDE

Using the temperature dependent shadow moiré technique developed at Georgia Tech, electronics manufacturers have applied the technology to evaluate substrate/package behaviors prior to production. The advantage being that those designs that exhibit severe or adverse warpage behavior during thermal processing can be identified prior to mass production. By pre-qualifying the warpage behavior of substrates/packages, manufacturers can further reduce the likelihood of defects that result in costly rework. In addition, high ppm defects due to adverse warpage behavior can cost manufacturers lost time and money from expensive diagnostic studies, flow-line downtime, scrapped components and delayed lot shipments.

Traditionally, engineers have looked at warpage behavior and its evaluation from a perspective of magnitude. Specifically, general guidelines and/or limits of acceptance have been quantified in terms of a single measured value as being the basis for acceptance or rejection. Typical (generic) industry and standards terms used to characterize the magnitude of warpage are presented below:

Printed Circuit Boards:

Bow – Quantified in terms of percentage. Calculated by dividing the magnitude of displacement along the edge of the board by the length of the edge.

Twist – Quantified in terms of percentage. Calculated by dividing the magnitude of displacement of 1 corner (holding the other 3 corners in the same plane) by the length of the diagonal of the board.

Chip-Carriers or BGA Packages:

Coplanarity – Quantified in terms of absolute magnitude. Calculated by determining the difference between the highest point and lowest point on a substrate/package.

Each of these parameters seeks to establish a threshold of acceptance based upon a measured magnitude of displacement. Historically, the analysis of substrate or package displacement magnitude has performed quite well. In any test/inspection environment it is ideal to reduce the information collected to a single value upon which a decision can be made. Bow, twist and coplanarity each provide a single value that enables this to occur.

Temperature dependent shadow moiré can be used to provide measured values of bow, twist and coplanarity at room temperature and during thermal loading. The unique advantage of thermal loading enables engineers to see the magnitude at such key temperatures as the glass transition point (Tg), eutectic point of solder (183 heating and cooling for tin-lead solder), and peak processing temperatures. The ability to determine the magnitude of displacement at these temperatures has proven to be of significant value – especially when compared to only pre-process and post-process measurements.

In the application presented, a 40 mm PBGA is to be reflow soldered to a multi-layer PCB. Room temperature measurements of the BGA and PCB bond pad area have acceptable coplanarity values prior to reflow processing. However, first article production runs experienced a high occurrence of interconnect failures. Investigation of warpage behavior of the BGA design and the PCB design during thermal processing was undertaken using phase-stepping shadow moiré technique.

Maximum vertical offset of the two surfaces for soldering was seen to be 10.0 mils (254 μm) for the BGA and 5.0 mils (127 μm) for the PCB bond pad area. These maximum values occurred at the peak temperature of 225 C. Allowable displacement magnitude was specified at 5.0 mils (127 μm). As evidenced by the data taken during thermal loading, the coplanarity/warp tolerance of the two independently behaving systems is well exceeded. The magnitude of warp directly contributed to a solder defect – in this case, a solder bridge in the pin 1 location.

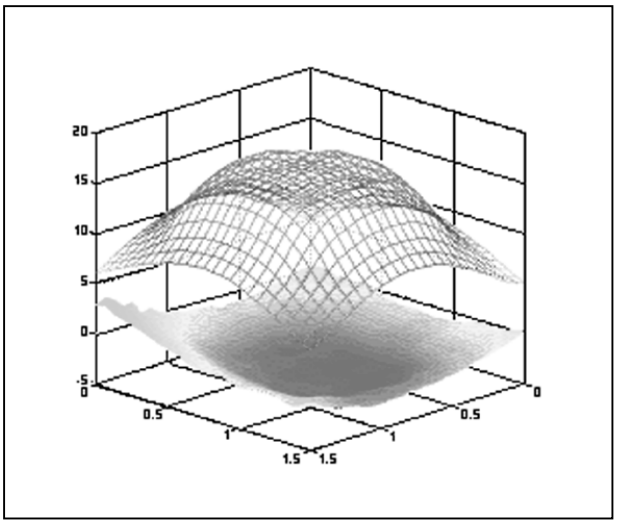
To evaluate the magnitude of displacement, both the PCB (data presented for the bond pad area only) and the PBGA were subjected to the prescribed reflow profile. The PCB and the PBGA were tested separately. Data for each part was plotted and then the 3D graphs were superimposed in order to qualitatively and quantitatively see the seating plane created between the two interconnect surfaces. An arbitrary offset of 5 mils (127 μm) for the two surfaces was selected for plotting purposes.

Figure 2 shows data for the PCB and PBGA at 225 C peak heating. It is at this point in the process that the maximum displacement occurs for the two surfaces. At this point, the solder is viscous and the balls have elongated in order to maintain connectivity between the solder bond pads on the PCB and the PBGA. This is true for over 90% of the solder balls for this full area array device. What is clear from the data is that the corner regions of the interconnect region are not being 'stretched' or elongated. As a result of the specific mechanical behavior of the PBGA and PCB and the tensile/pulling force of the elongated solder balls, the corner areas are actually coming under compressive forces. The compressive forces in the corners – created by the pulling force of a majority of the solder columns and the 'pinching' of the PCB and PBGA in these areas – was strong enough to cause the solder ball at the pin 1 location to bridge with the neighboring solder ball.

Figure 3 shows the data set for the PCB and PBGA at 183 C cooling. It shows that the PBGA has dramatically reduced the magnitude of its warpage relative to the magnitude at

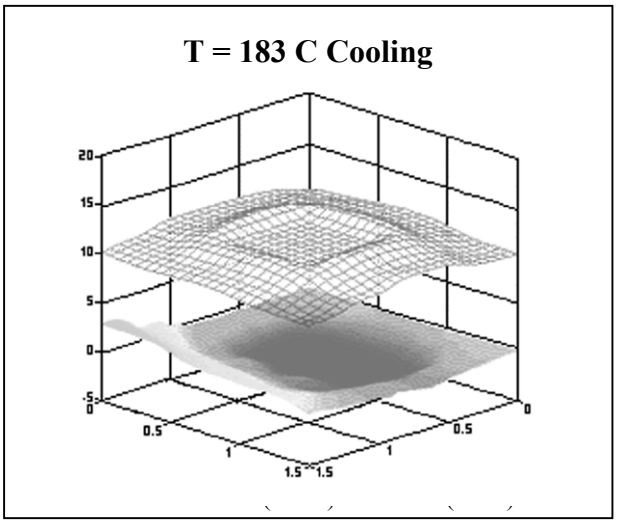
peak temperature. It is now coplanar to within 4.0 mils (102 µm). The solder balls that were elongated at peak temperature have now returned to their spherical intent due

Figure 2: Thermally loaded PBGA and PCB substrate.



to the fact that the interconnect region is now within design tolerances. This being the freezing point of tin-lead solder, a good connection is made. Unfortunately, the damage has already been done and it is evident in the form of a non-acceptable defect – a solder bridge. This assembly must be reworked in order to be fully functional.

Figure 3: Thermally loaded PBGA and PCB substrate.



In this example a pre-production evaluation/qualification of temperature dependent behaviors could have alerted the assembler of the likelihood of defects due to the magnitude of warpage experienced during thermal loading.

LOCATION

A second case study exposes the risk of using warpage magnitude as a sole gauge for limiting mechanically induced defects. While magnitude is indeed important to warpage characterization, it is equally important to evaluate the location of warpage. In this study, a packager attempted to evaluate the effects of varying sizes of encapsulant molds for a PBGA device. For a 35 mm laminate chip-carrier, devices with encapsulant dimensions of 25 mm, 27 mm and 30 mm were constructed. All other construction parameters were held constant. Samples of each encapsulant dimension were evaluated for maximum warpage magnitude during thermal processing using temperature dependent shadow moiré technique. The shadow moiré data was then used to predict and later correlate assembly (device to PCB) yield based upon warpage magnitude.

Results from the shadow moiré testing are presented in Figure 4. It is seen that the maximum displacement (along diagonals of the data set) was indeed impacted by the encapsulant dimension. Notably, the 27 mm and 30 mm designs were roughly twice as great in magnitude as the 25 mm design.

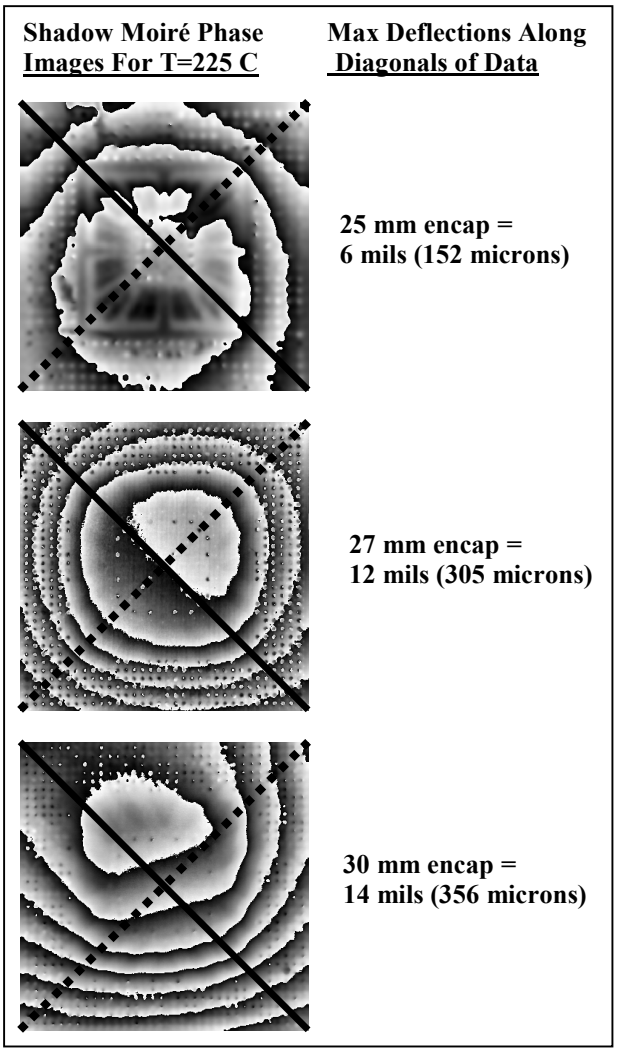
Based upon this data, it was predicted that the 27 mm and 30 mm designs were likely to experience warpage related defects during assembly to the PCB. During first article production runs, results (yields) were as expected for the 25 mm encapsulant design – no defects occurred. For the 27 mm and the 30 mm designs, the results were quite different. Even though the magnitude of maximum displacement was within 2.0 mils (50 microns) for the two designs, the first article yields were completely opposite. The 27 mm encapsulant design achieved a zero defect run, whereas the 30 mm encapsulant design produced a significant number of opens/shorts.

In-depth analysis of the assembly failures for the 30 mm design revealed an important correlation. The defect occurrence during assembly for the 30 mm design was consistently found in the innermost row of solder balls. The shadow moiré data sets were revisited for further analyses. This time, instead of analyzing the displacement of the package along the diagonals, the displacement of the package along the innermost row and outermost row of solder balls were evaluated.

Figure 5 shows the data sets for each of the three package designs along the outermost row of solder balls. As on can see, the magnitude of displacement along this row is quite consistent between each design.

Figure 6 shows the data sets for each of the three package designs along the innermost row of solder balls. Here, it becomes clearly evident that the 30 mm encapsulant design is distinctly different in behavior from the other two designs. The magnitude of displacement at this critical location is significantly greater than the other two designs. This analysis clearly shows why defects in the 30 mm design were occurring and why defects in the 27 mm design were not occurring – despite their very similar warpage magnitudes as defined by the initial pre-production evaluation.

Figure 4. Package deformation analysis – magnitude.



TYPE

Characterizing warpage for a substrate/package can further be examined with respect to the type of displacement that is present. The simplest and most prevalent occurrence is negative (concave) or positive (convex) curvature. Other more complex types of curvature include twist and waviness.

Using shadow moiré technique in a room temperature application, a series of flex-BGA substrates were analyzed for maximum warpage values. The substrates were 6-up arrays of 23 mm X 23 mm polyimide flex tape with a copper frame. In effort to reduce scrap – because there is no rework on package assembly – the manufacturer set a pass/fail threshold (absolute) of 3.0 mils (100 µm). The method of chip attach was direct. Again, magnitude alone was selected as the parameter for pass/fail of each area.

Each of the 6 die attach areas on a strip was measured for coplanarity prior to entering the package assembly flow line. Those areas in excess of the threshold were 'x-outs' and subsequently no assembly was performed in these regions. Approximately 625 data points for each die attach area were collected for analysis. A regression plane was determined and coplanarity was calculated as the difference between the highest point and the lowest point in the matrix.

Figure 5. Outer-most row of solder ball pads are analyzed for maximum deflection.

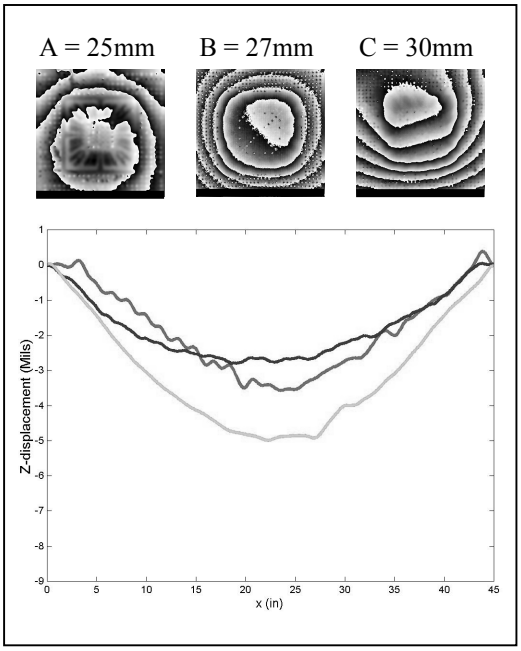


Figure 6. Innermost row of solder ball pads are analyzed for maximum deflection.

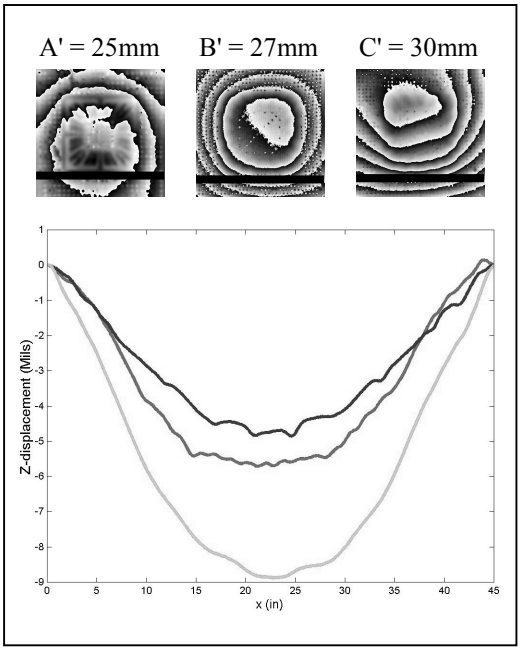
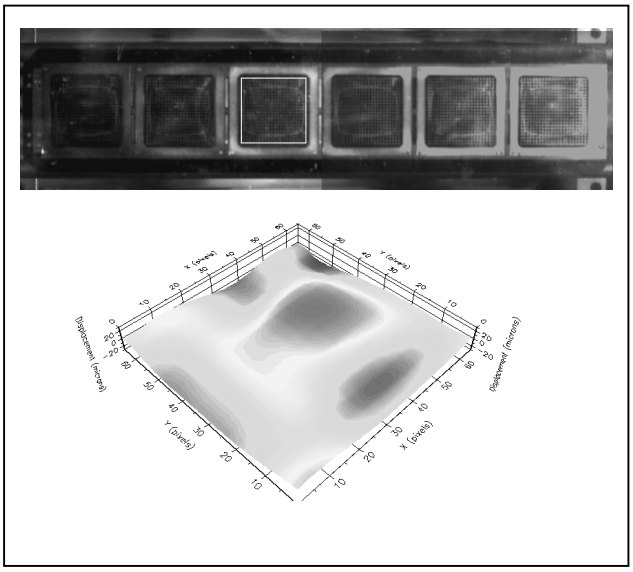


Figure 7 shows the flex-BGA substrate (typical) and its resulting 3D surface plot from shadow moiré data. Coplanarity is given for the die attach area (22 mm X 22 mm inspection area). In this evaluation, an approximate 12% of die attach areas failed the 3.0 mil coplanarity limit.

These were subsequently omitted from die attach processing. Those sites on strips that passed the inspection parameter were then processed to completion.

Figure 7. Flex-BGA strip warpage analysis with shadow moiré technique.



Post-processing test and inspection revealed that defects existed in roughly 5% of the lot. Additional analysis of the pre-production coplanarity data yielded a strong correlation between the 5% fallout and coplanarity values (relative) between –3.0 mils (-51 µm) and –1.7 mils (-43 µm). Approximately 80% of the interconnect (die – flex) defects had pre-production coplanarity values between –3.0 mils (-51 µm) and –1.7 mils (-43 µm).

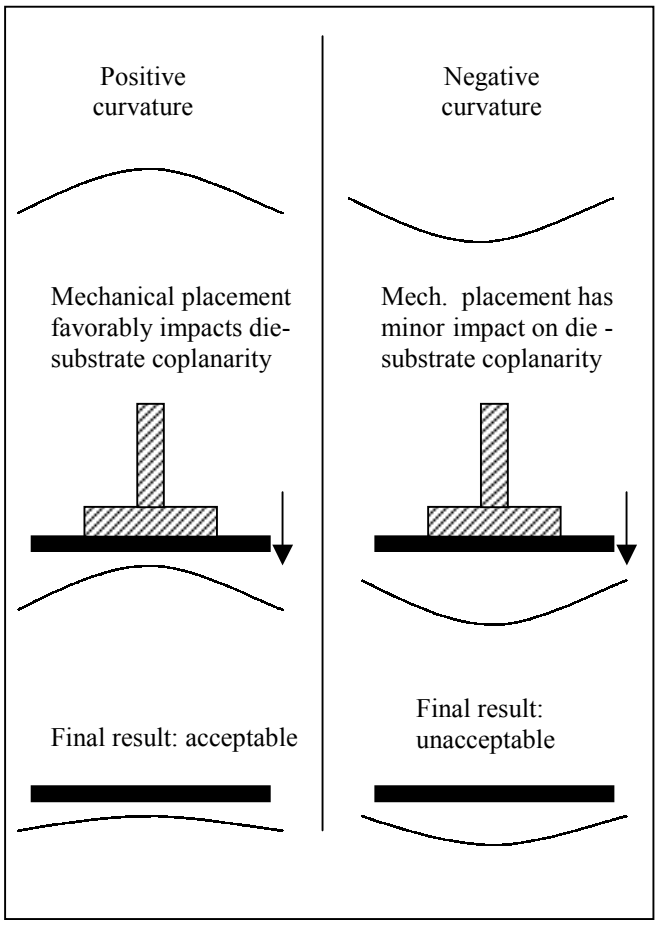
It was theorized and concluded that dependent upon the type of curvature – positive or negative – independent thresholds for pass/fail should be prescribed. It was determined that the amount of positive curvature that could be tolerated without consequence was close to 2 times greater in magnitude than that for negative curvature. Implementing this conditional threshold further increased the number of die attach areas that would have failed the pre-production inspection (approximately another 4%); however, it would have significantly decreased the number of experienced defects due to interconnect failure (approximately 80%).

Figure 8 shows that the mechanical action of die placement actually aids in correcting excessive positive curvature. Additionally, it shows that mechanical action of die placement is equally incapable of assisting negative curvature.

ADVANCED CHARACTERIZATION AND RELIABILITY

It is important to attempt to tie together the too-often independently treated realms of interconnect and reliability - especially when warpage characterization is concerned.

Figure 8. Schematic presentation of flex-substrate curvature and how mechanical placement of the silicon die can favorably impact die-substrate coplanarity.



Traditionally, the emphasis on reliability is applied during development and qualification of a new package and/or assembly design. Upon reaching desired design and performance standards, product is transferred to volume production where reliability is assumed and successful interconnect (i.e. yield) is monitored and driven relentlessly.

The case studies presented previously on warpage magnitude, location and type have focused primarily on interconnect. In each of these examples, we analyzed relatively clean failures such as opens and shorts due to adverse mechanical behaviors. More difficult analysis of package/assembly reliability issues related to mechanical behaviors is an equally critical area for investigation. The ability to accurately predict and quantify product reliability will only intensify with new processing related challenges such as bromine-free laminates and lead-free solders.

In a study conducted by Siemens AG it was concluded that the type of interposer material selected for CSP assembly must be measured for warpage behavior (magnitude and type) in order to determine the level of irreversible deformation. This irreversible deformation is a direct contributor to the reliability of a selected package design. It

was shown that the solder balls are largely responsible for any stress created by mechanical behavior deformations below 183 C cooling on the cool down of reflow processing. Data was presented that indicates 70-90% of deformation can be estimated as irreversible deformation (for flex, rigid and ceramic substrates) [6].

Combining the observations of Siemens AG with the observations in this study, it can be hypothesized that warpage magnitude, location and type can reach beyond impacting interconnect and into reliability. Each of these areas of advanced warpage characterization can potentially provide a means for advanced study of irreversible warpage and its impact on reliability.

While the study at hand did not embrace this hypothesis for investigation, the author felt it necessary to present the parallels of the two independent papers for consideration.

CONCLUSIONS:

1. Magnitude of warpage is a valid, but not comprehensive means for characterizing warpage.
2. Thermal loading of packages/substrates can significantly alter the magnitude of warpage behavior.
3. The locations of warpage on a substrate/package can significantly impacts the ability to perform successful interconnect processing.
4. Characterizing the type of curvature can provide further value in identifying substrates/packages with high probabilities of incurring warpage related defects.
5. It is hypothesized that evaluation of location and type in addition to magnitude of irreversible warpage could further benefit the study of solder-joint and package reliability.

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