EFFECT OF PACKAGE WARPAGE AND COMPOSITE CTE ON FAILURE MODES IN BOARD-LEVEL THERMAL CYCLING

Andrew Mawer, Paul Galles, Mollie Benson and Burt Carpenter
NXP Semiconductors, Austin, Texas USA
andrew.mawer@nxp.com

Neil Hubble
Akrometrix, Atlanta, Georgia USA
NHubble@akrometrix.com

ABSTRACT
Increasingly, demonstrating adequate reliability performance for a given packaged integrated circuit (IC) while mounted to a printed circuit board (PCB) that represents as closely as possible the final application is a requirement from both IC suppliers themselves and their Tier 1 customers. This combined with the ongoing miniaturization of electronic packages in both footprint and height, sometimes to the detriment of board-level reliability (BLR) thermal cycling (TC) performance, has put more scrutiny on the robustness of the interconnection from the package to the PCB. Well known byproducts of miniaturization that can lead to decreased solder joint interconnect fatigue lifetimes in BLR TC on BGAs, for example, include finer pitches with smaller solder spheres, larger die to package ratios and thinner laminate substrates. Not only is the fatigue lifetime in BLR TC examined closely, but also the specific failure modes and location. Additionally, depopulation of certain BGA locations to facilitate package substrate or PCB routing can affect BLR cycles to failure and influence the location of first failure.

This paper will give examples of the BLR TC failure modes and locations of various package test vehicles that were designed to attempt to correlate those failure modes to the in plane CTE and out of plane warpage behavior of those packages. BLR TC results will be presented in Weibull format along with failure analysis using both cross-sectioning and dye penetrant analysis.

Package CTEs were measured using Digital Image Correlation (DIC) and package warpage over approximately the same temperature range as TC was measured using CoolMoiré, a Shadow Moiré technique that brings the sample to temperatures as low as -55ºC. The results show that by knowing both the warpage and CTE behavior of packages, the board mounted TC failure location, and to lesser extent, the relative performance, can be better understood. The two package types that will be studied are flip chip PBGA (FC PBGAs) and overmolded, wire-bonded PBGAs with various die sizes.

Key words: Solder Joint Reliability, SJR, Board Level Reliability, BLR, Coefficient of Thermal Expansion Mismatch, CTE, TherMoiré, CoolMoiré, Shadow Moiré, Interferometry, Digital Image Correlation, DIC, Package Warpage, Ball Grid Array, BGA

*Originally published at SMTAI 2018

INTRODUCTION
Failures in BLR TC are traditionally been thought to be driven primarily by the CTE mismatch between the silicon IC, the package materials, PCB and the solder itself [1-3]. These mismatches cause the package to undergo both out of plane warpage and in plane expansion and contraction as it goes through temperature excursions. Similarly, the PCB is also going through in plane expansions and contractions, and if its construction is asymmetric about the mid-plane due to factors such as unbalanced copper, it may also experience out of plane warpage like that of a package. The out of plane warpage of the package tends to put various solder interconnects in alternating or cyclic tensile and compressive stress while the in-plane expansion / contraction or CTE mismatch to the PCB tends to result in a shear stress on the affected interconnects. These factors can also work in combination on a given interconnect depending on the package construction. Other factors that influence how a package warps during temperature cycles are the individual CTE's, Young's moduli and Tg's of the materials (i.e., die attach, mold compound, substrate including dielectric and soldermask, lid adhesive, thermal interface material), die thickness, substrate construction and thickness [4-5].

PACKAGE TEST VEHICLES
Six sample types representing a wide range of pitches, body sizes, die sizes, die to package interconnection technologies and substrate constructions were designed and built for this study. They are listed in Table 1 and will be referred to by the letter designations A through F throughout this paper. Types A through D were wire-bonded and molded BGAs and types E and F were flip chip BGAs. All the wire-bond parts were molded to the substrate edge such that the mold size and substrate size were identical. Wire-bonded part substrate thicknesses ranged from 0.21 to 0.30 mm. Both flip chip BGA parts employed a footed copper lid that covered the die and attached to the perimeter of the substrate. Besides a perimeter adhesive, the lid was attached to the die using a low modulus thermal interface material (TIM). Flip chip part types E and F had the largest body sizes, contained the largest die and had substrates that were 0.68 and 0.77 mm thick, respectively.

Table 1. Attributes of the six packages used in this study. A-D are molded wire-bond BGAs and E-F are Flip Chip BGAs.

Pkg	Package Type	Pin Count	Body Size (mm)	Die Size (mm)	Die to Pkg Ratio	Substrate Thickness (mm)	Pitch (mm)	Comment
A	Molded WB PBGA	141	10x10	6.12 x 6.92	0.42	0.30	0.65	Largest die to package ratio
B		141	10x10	No Die	N/A	0.30	0.65	No die, but die attach is present
C		257	14x14	8.4 x 7.4	0.32	0.30	0.8	Largest wire-bond BGA die
D		393	14x14	4.08 x 4.08	0.08	0.21	0.5	Smallest die to package ratio
E	Lidded FC PBGA	1313	29x29	13.12x12.82	0.20	0.68	0.75	Depop row next to die edge
F		1932	45x45	16.19x15.05	0.12	0.77	1.0	Largest die and body size

The BGA side of all the parts that were studied are shown approximately to scale with the die outline overlaid in red in Figure 1. Note that part type B was the same as A except for type B had no die present. As can be seen in Figure 1, besides other attribute differences, the parts also represented a range of BGA sphere depopulation schemes.

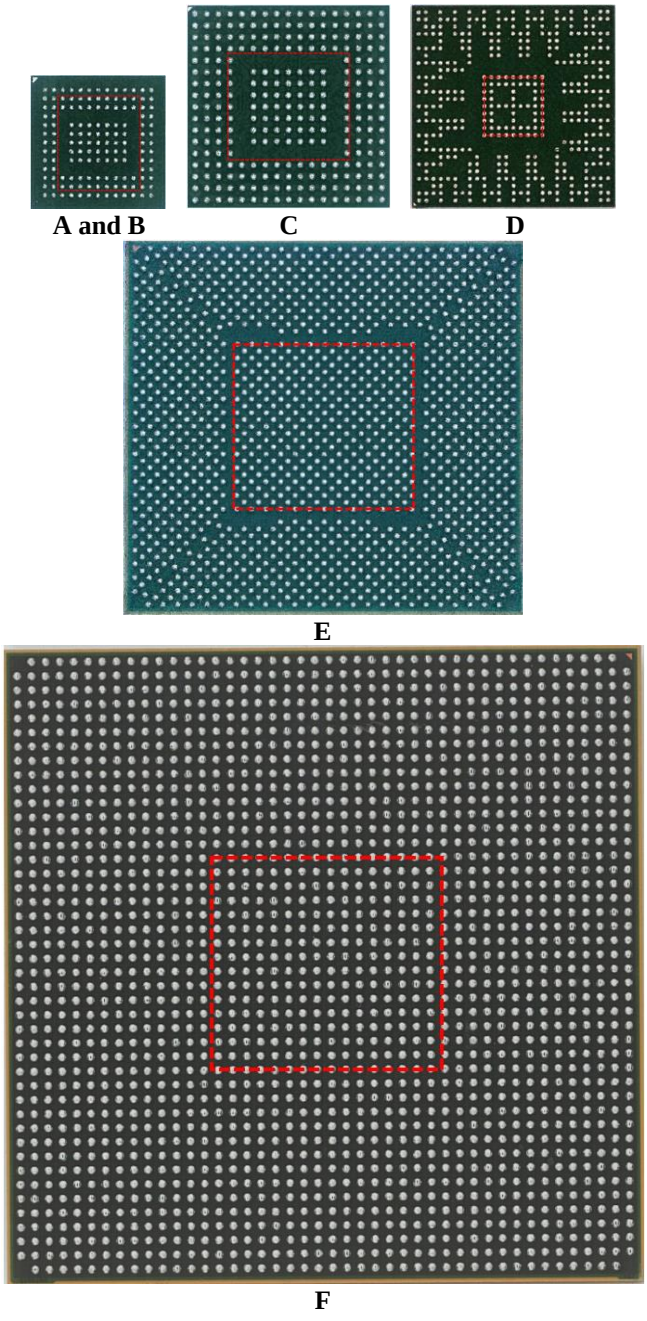


Figure 1. Bottomside images of the five BGA configurations used for this study. Images are approximately to scale.

BOARD-LEVEL THERMAL CYCLING TESTING

Daisy-chain versions of each of the six part types were soldered down to PCBs using halide free, no-clean SAC305 solder paste and a peak reflow of approximately 240ºC and subjected to continuously, in-situ monitored thermal cycling from -40 to 125ºC until at least 75% of the packages recorded a failure. The primary -40 to 125ºC thermal cycle, which is shown in Figure 2, was carried out at a controlled ramp rate of 11ºC/min with 15 min ramp times and dwell times in a single chamber resulting in a one hour total cycle. Part type F, which is targeted primarily at telecom and networking applications, was additionally cycled from 0 to 100ºC with both ten minute ramp and dwell times. Part types A and B were the only parts that were subjected to a thermal shock cycle. This cycle was also -40 to 125ºC, but employed a dual chamber where the boards were shuttled from the temperature extremes in a few seconds. All the PCBs used organic solderability (OSP) surface finish and non-soldermask defined (NSMD) pads that were 1:1 with the package SMD pad diameter.

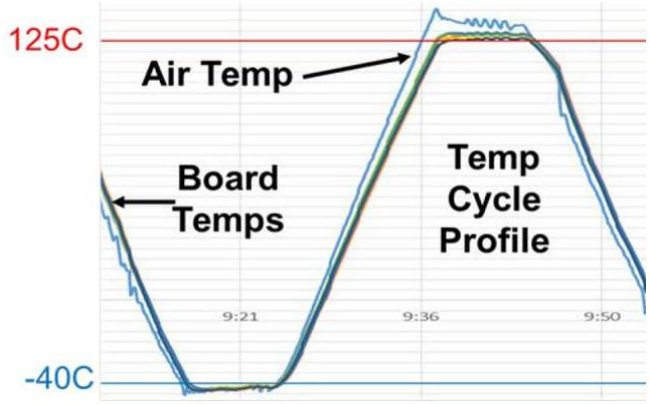


Figure 2. Actual controlled ramp rate, single chamber one hour -40 to 125C BLR temperature cycle profile with thermocouples affixed to the PCBs and monitoring the air.

After each of the six part types achieved >75% failure, the PCBs were pulled from the chamber for data and failure analysis. The BLR cycles to failure data for all six part types were plotted on two parameter Weibull axes in Figures 3 through 7. For three of the part types, A, B and D, the data is plotted broken into 4two separate monitored regions. As Figure 1 demonstrates, the center versus outer or perimeter spheres were monitored separately on parts type A and B during BLR. Part types A and B are shown on the same Weibull since they were the same package with and without die. Since the number of samples with no die (type B) was

small, two sphere alloys and two package substrate surface finishes were combined to create the graphs in Figure 3. Although this resulted in relatively low correlation coefficients (r^2), the resulting trends are evident. Quite unexpectedly, the no die parts (type B) failed almost 2x earlier than the parts with die (type A) when comparing characteristic life (eta or η). Additionally, the failure mode shifted from the outer row failing first with the die present to the inner joints failing first with no die. Comparing just the center joints, there is a remarkable 7X difference in eta. Using either cross-sectioning or dye penetrant analysis, Figure 8 shows exactly where first failure was recorded for each of the six part types. For part A, failure was generally on the innermost row of the outer perimeter rows of spheres and for part type B with no die, failure was on the centermost sphere of the entire package. Part type C, which has cycles to failure data plotted in Figure 4, had a solder joint failure location identical to part type A. Since type C had a coarser pitch, larger sphere diameter, larger body size and lower die to package ratio compared to A, it performed better overall. Part type D, which had the thinnest substrate and the smallest die size of all the parts studied, was monitored with three nets per part: 1) corner spheres, 2) center spheres and 3) outer spheres excluding the corners. These three nets are plotted separately in Figure 5 along with all the data combined. As can be seen in the plot, the corner spheres failed first on this part and the remaining outer spheres only recorded one failure by the time the test was terminated. Figure 8 shows an example of a fractured corner spheres for part type D. Note the apparent minimal damage to the neighboring sphere in this cross-section.

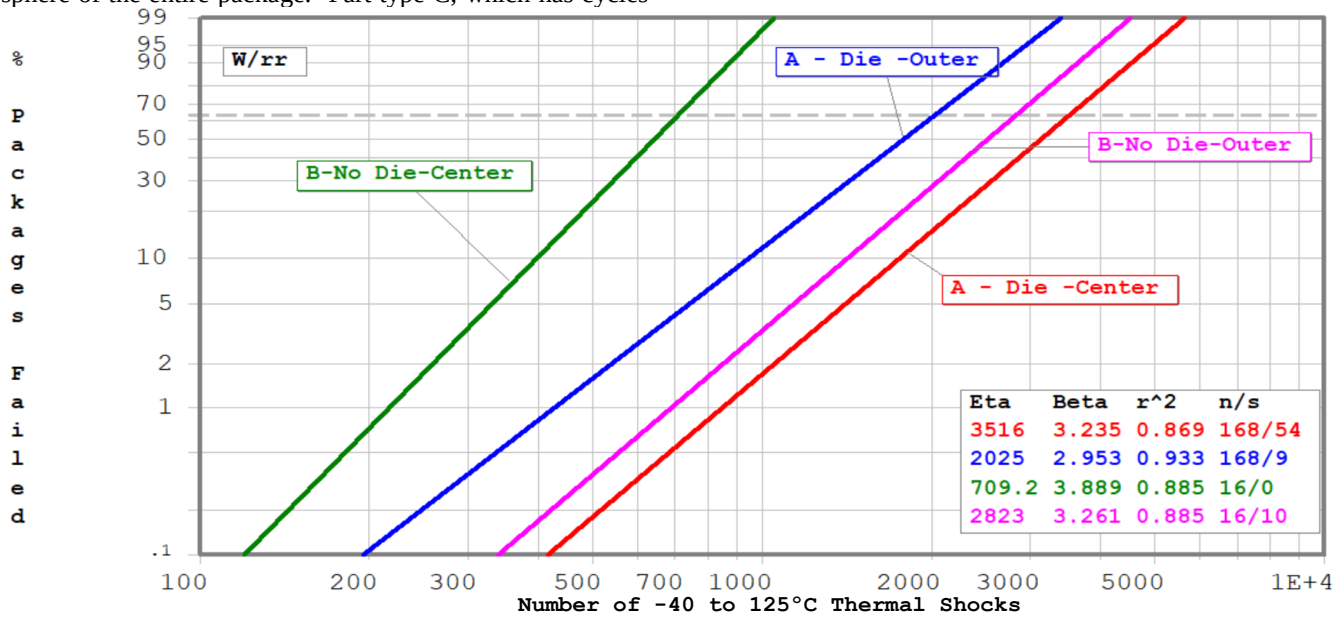


Figure 3. Two parameter Weibull plot of the BLR cycles to failure data for package Type A and B which is the same package type with silicon die present and without any die. Data is broken up by outer and center solder joints.

*Originally published at SMTAI 2018

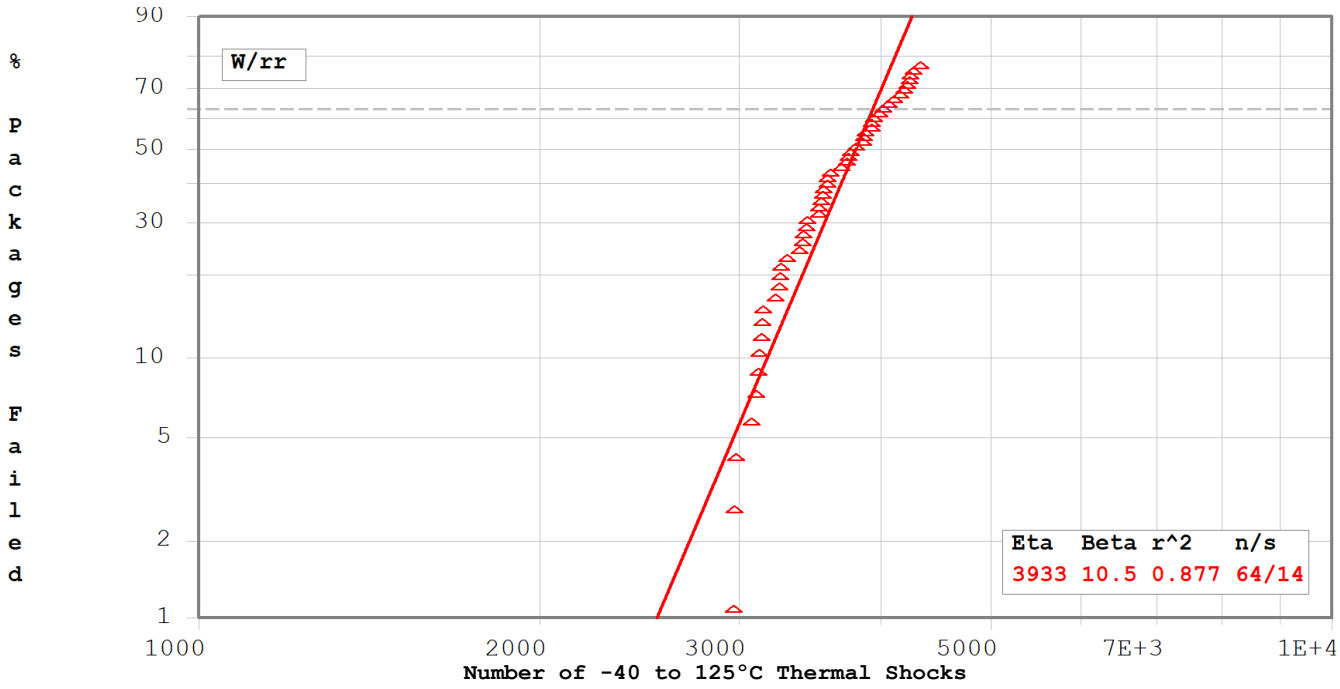


Figure 4. Two parameter Weibull plot of the BLR cycles to failure data for package Type C.

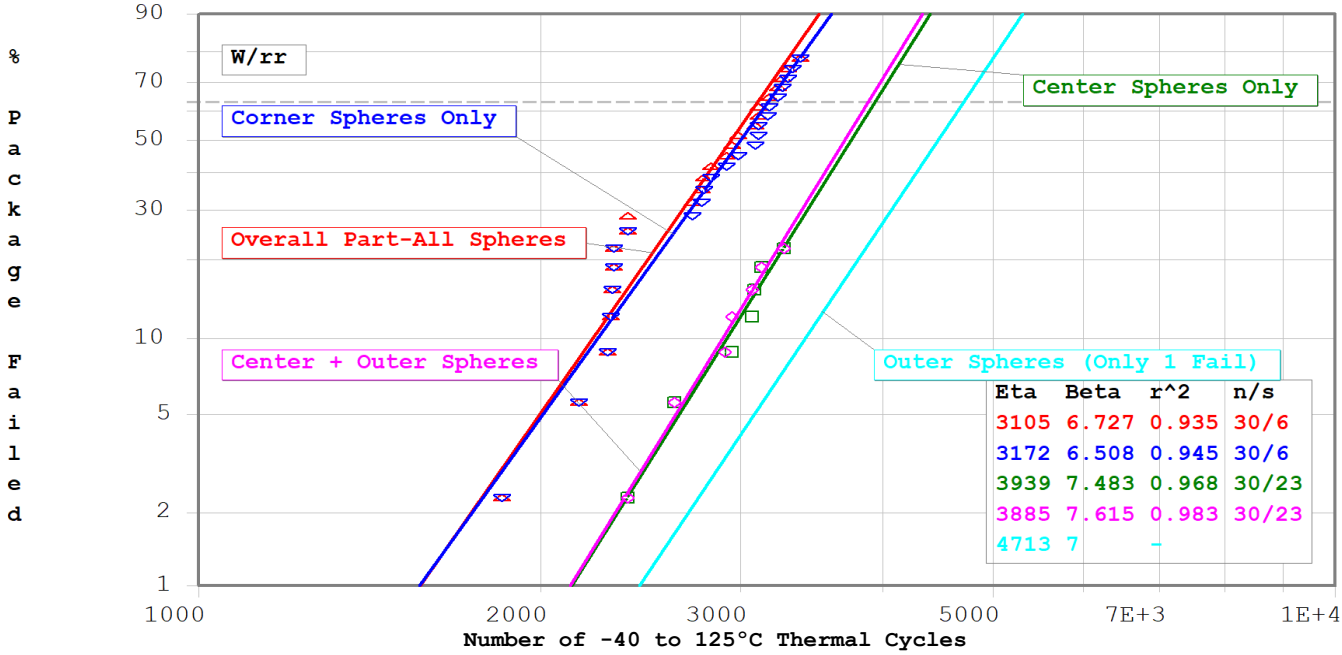


Figure 5. Two parameter Weibull plot of the BLR cycles to failure data for package Type D. Package was broken into three nets for monitoring: center, outer and corner. As can be seen from the plot, corner spheres were responsible for almost all of the first failures.

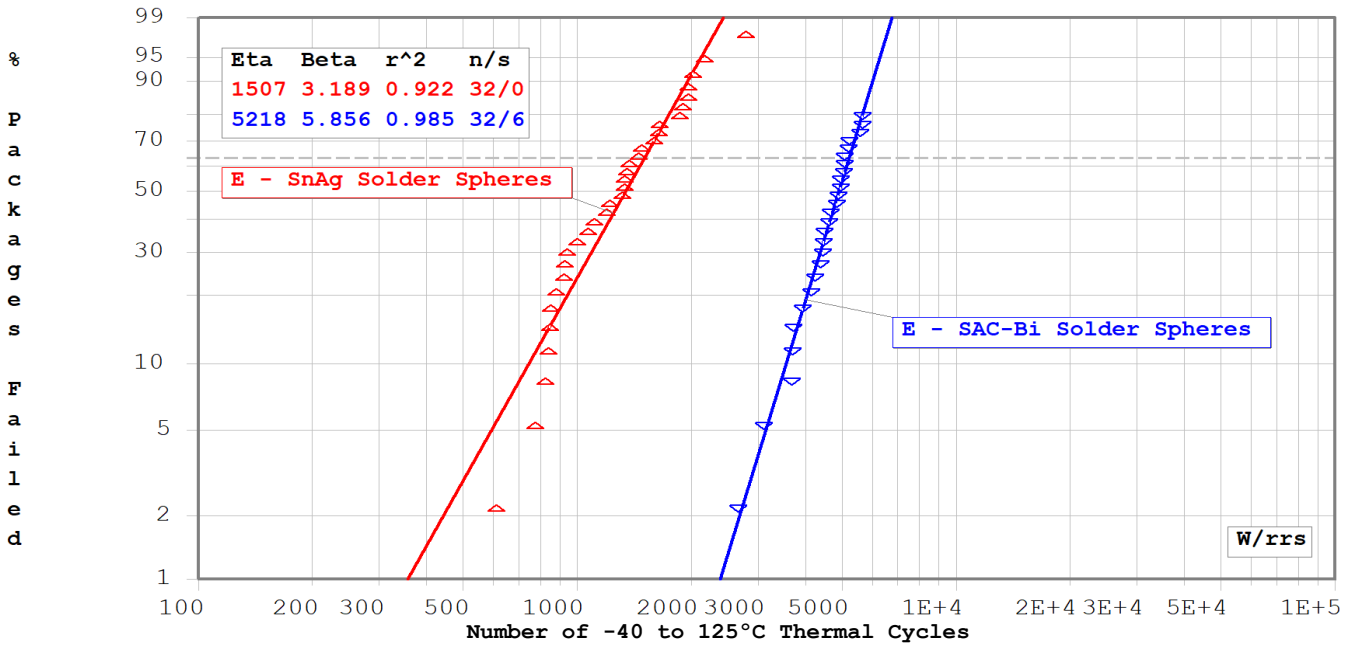


Figure 6. Two parameter Weibull plot of the BLR cycles to failure data for package Type E. Package was tested with both eutectic SnAg spheres and SAC spheres containing Bi which greatly improved cycles to failure.

The BLR data for the two flip chip parts is plotted in Figures 6 and 7. Those two parts had very similar construction with a full footed copper lid and a substrate that was greater than 2× thicker than the wire bond parts. Referring back to Figure 1, part type E, which had a 0.75 mm staggered pitch, had a depopulated row of spheres that is located right outside the die edge. For that part, the sphere in the corner of the row inside the depopulated row, which was coincident with the die corner, consistently failed first. Additionally, the recorded cycles to failure for this part using a SnAg eutectic (96.5%Sn/3.5%Ag by weight) sphere alloy was 600 cycles. This part was also run with stiffer and more fatigue resistant bismuth containing SAC alloy that increased both the cycles to first failure and the eta by 4× as can be seen in Figure 6 [6]. Lastly, data for part type F, which was a fully populated array with the thickest substrate tested at 0.77 mm thick, is shown in Figure 7. This is the only part in this study that was tested in both -40 to 125ºC and 0 to 100ºC single chamber cycling. For this part, the center sphere was observed to fail first regardless of the cycling condition. This is evident in cross-section in Figure 8 with fatigue fractures seen propagating close to the package pad on both center spheres.

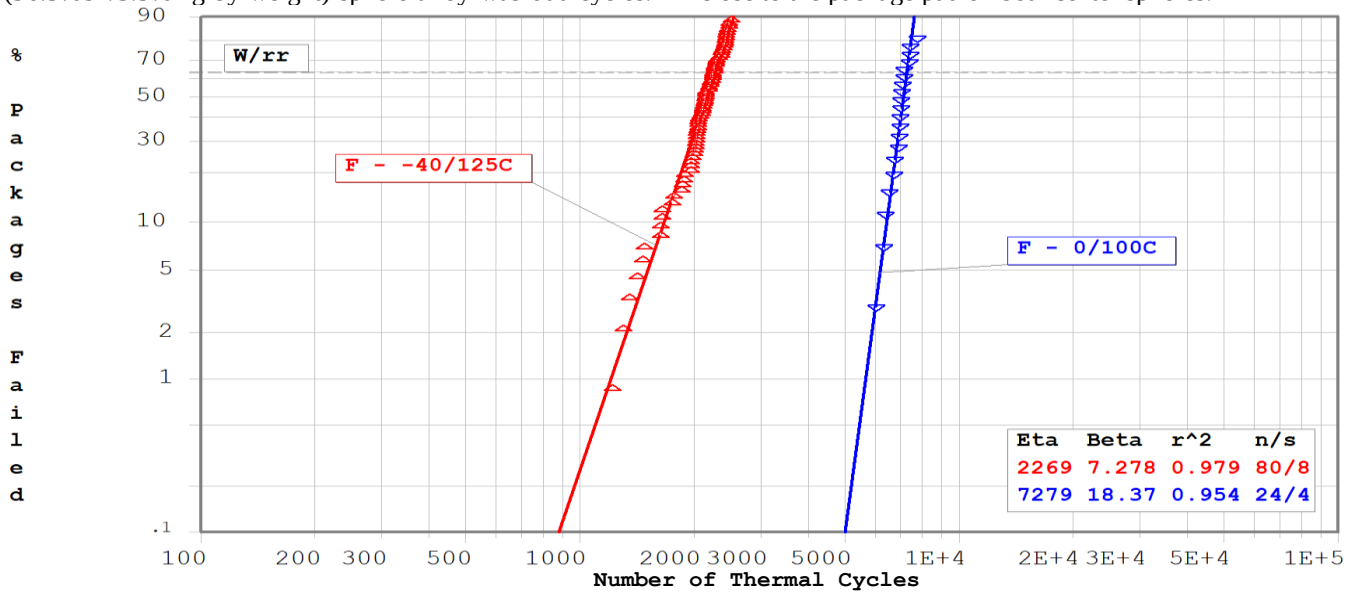
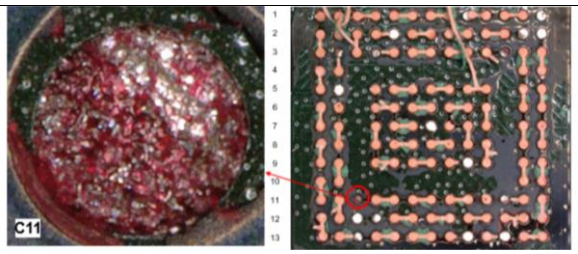
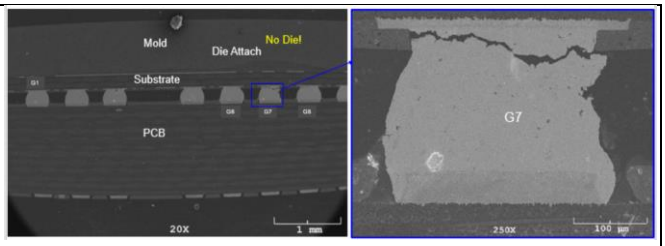


Figure 7. Two parameter Weibull plot of the BLR cycles to failure data in two cycling conditions for package Type F.

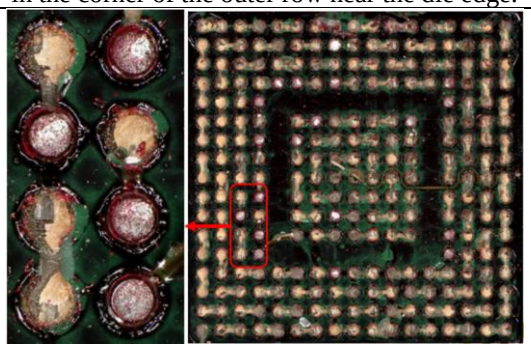
*Originally published at SMTAI 2018



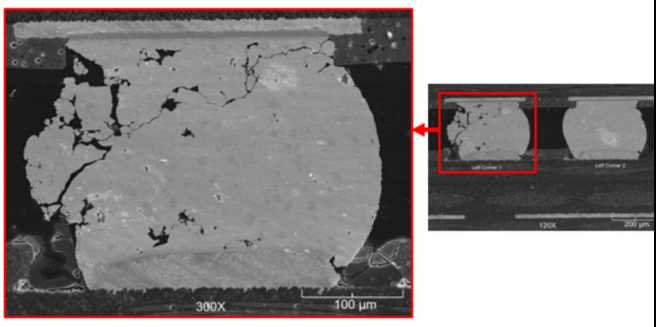
Part A – Dye penetrant image showing first failure in the corner of the outer row near the die edge.



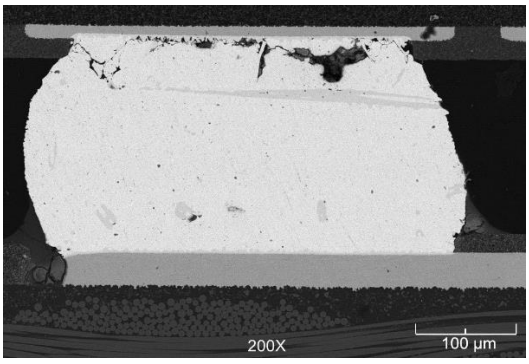
Part B – Cross-section showing failure in the exact center sphere when no die was present.



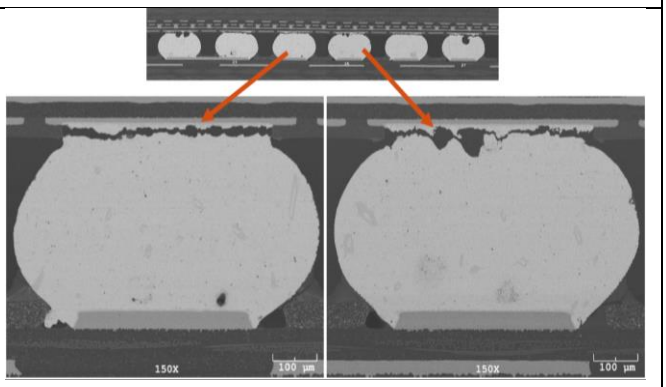
Part C – Dye penetrant image showing first failure in the corner of the outer row near the die edge.



Part D – Cross-section showing failure in the corner sphere with almost no fracturing in the adjacent sphere.



Part E – Cross-section showing failure in the solder joint at the corner of the die adjacent to the depopulated row.



Part F – Cross-section showing failure in the center spheres on this fully populated part.

Figure 8. Cross-section and dye penetrant images showing location of the first solder joints to fail on part types A through F.

MEASUREMENTS OF PACKAGE OUT OF PLANE WARPAGE USING SHADOW MOIRĖ

Each of the package types in this study were measured for package out of plane warpage during a typical -40 to 125ºC BLR thermal cycle. The entire thermal cycle used for measurement including all the readpoints is shown in Figure 9. Note that even though the thermal cycle is from -40 to 125ºC, additional measurements were taken as cold as -55ºC and as hot as 150ºC. Three samples of each of the six package configurations were measured. Before each measurement the spheres were removed from the bottomside of the BGAs with solder wick, the bottom of the part coated with a thin layer of high temperature white paint and the parts baked at 125ºC for approximately four hours to ensure no delamination or popcorning. An example of a typical part after preparation is shown in Figure 10.

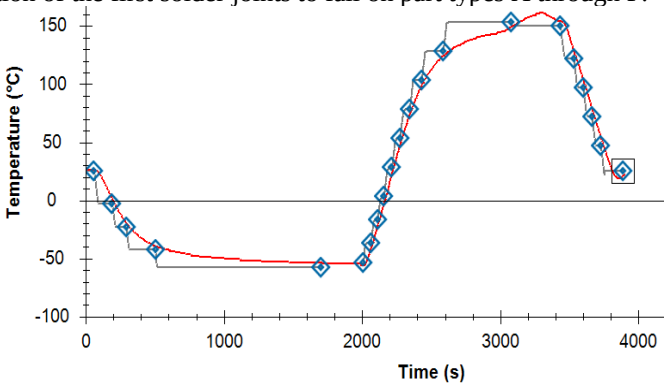


Figure 9. Temperature cycle shown with readpoints used for shadow moiré warpage measurement of the samples.

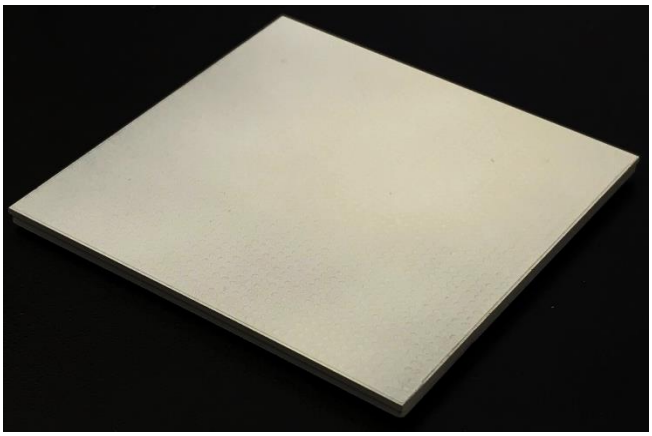


Figure 10. Bottomside of typical part after preparation for shadow moiré by removing the solder spheres and applying a white high temperature coating. Part type F is shown.

The technique used for measurement was shadow moiré which is a non-contact, full-field optical technique that uses geometric interference between a reference grating and its shadow on a sample to measure relative vertical displacement at each pixel position in the resulting image [7-9]. It requires a Ronchi-ruled grating, a white line light source at approximately 45 degrees to the grating and a camera perpendicular to the grating. Its optical configuration is shown in Figure 11. A technique, known as phase stepping, is applied to shadow moiré to increase measurement resolution and provide automatic ordering of the interference fringes. This technique is implemented by vertically translating the sample relative to the grating. In this case, a convective cooling module is added to the shadow moiré system to enable sub-room temperature readings. The resulting technique is called CoolMoiré. For the above room temperature portion of the BLR thermal cycle, convective heating is used to heat the sample.

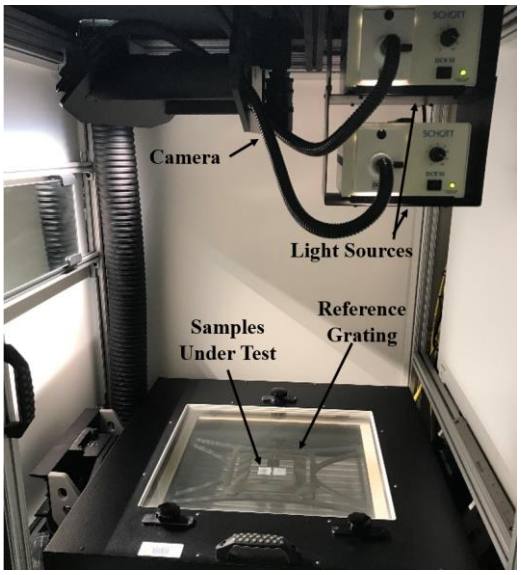


Figure 11. Shadow moiré configuration comprising of a camera, light source, grating and the samples under test.

The CoolMoiré results for all six part types are presented in Figure 12. Bottomside images for a representative part are given at the most relevant temperatures of 25, -40 and 125ºC. Below each image is the coplanarity at that temperature which is defined as the delta between the highest and lowest points on the sample. The data shown has not been filtered or smoothed in any way and the original BGA pad locations from which the spheres were removed are visible for each sample. For this reason, a portion of the listed warpage value, approximately 10 μm, can be assumed to represent the difference in height between the BGA solder pads and the soldermask over copper surrounding it. For all samples the maximum warpage recorded was at -40ºC and for most samples the minimum warpage was at 25ºC. There was a general trend with the two substantially larger flip chip parts (E and F) having the largest warpage. Most parts stayed relatively flat during the thermal cycle, especially A and B which only exhibited ≤ 10 μm of warpage change throughout the entire -40 to 125ºC range. The flattest part overall was part type B, which is not surprising since it contained no silicon. Silicon, with its CTE that is at least 5× lower than most package materials, is of course believed to be the largest driver of CTE mismatch and therefore warpage. Part types C and D, and to a lesser extent A, exhibited somewhat of a "saddle" behavior with two opposite corners warping upward at -40ºC. The most distinct behavior was exhibited by the flip chip parts (E and F) where the influence of the die CTE mismatch was very visible at 25 and -40ºC and was almost nonexistent at 125ºC. At 25 and especially -40ºC, the area in the center of the part appeared as a distinct depression.

Pkg	25ºC Initial	-40ºC	125ºC	Scale (μm)

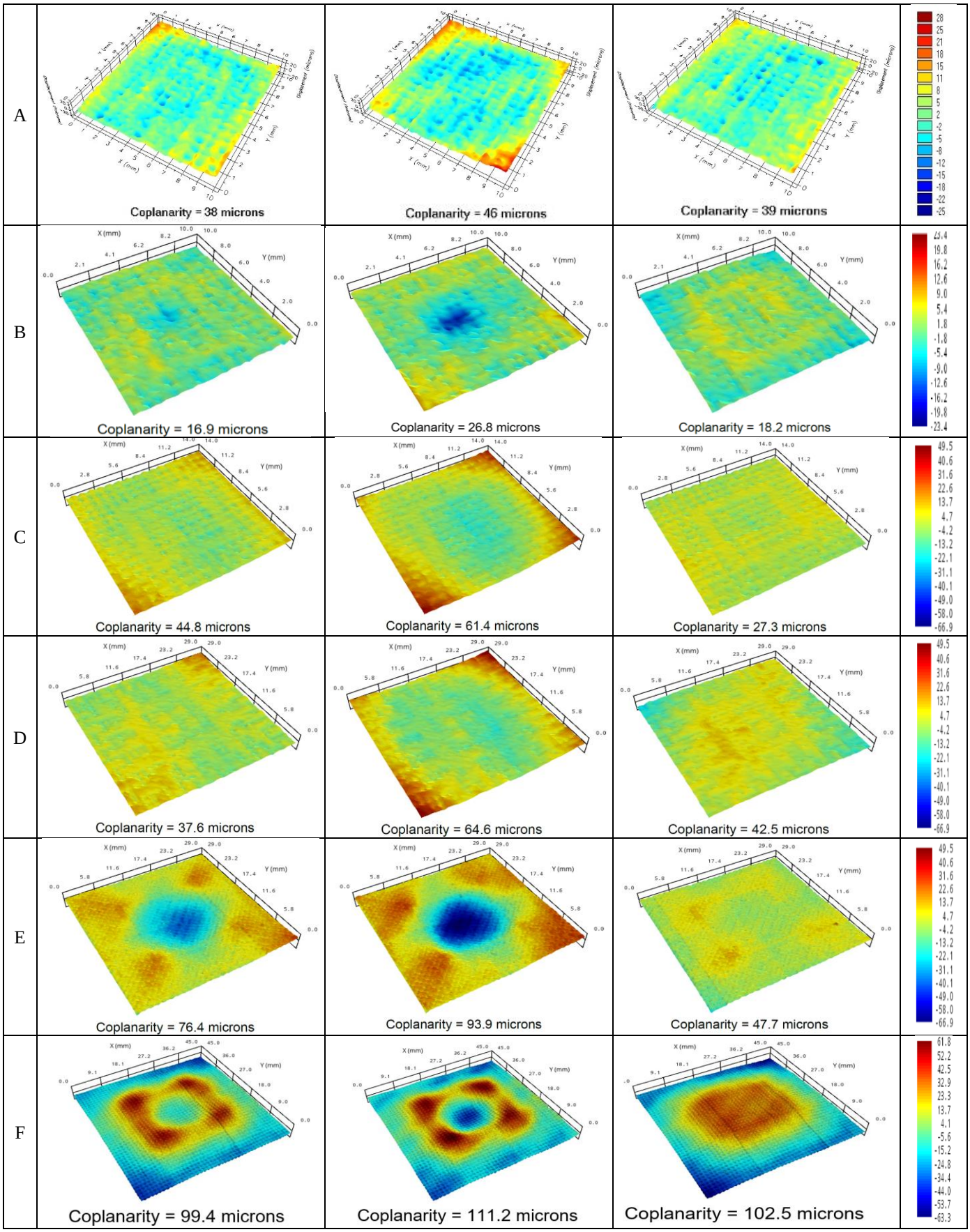


Figure 12. Bottomside package warpage measurements of all six BGAs at 25, -40 and 125ºC. Note scale in right column.

*Originally published at SMTAI 2018

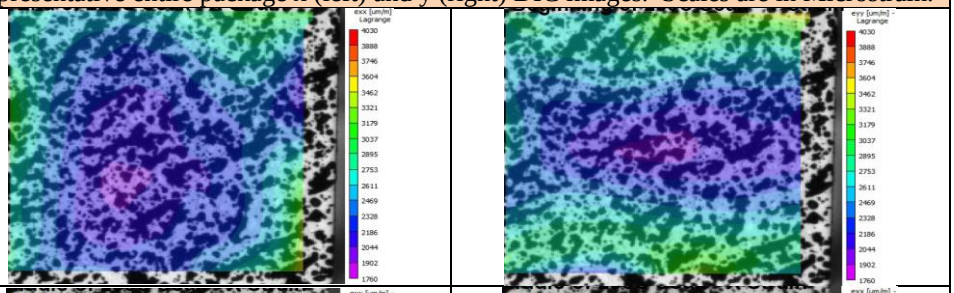
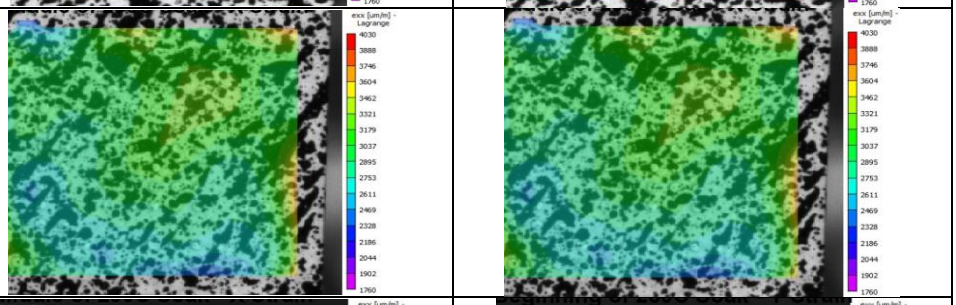
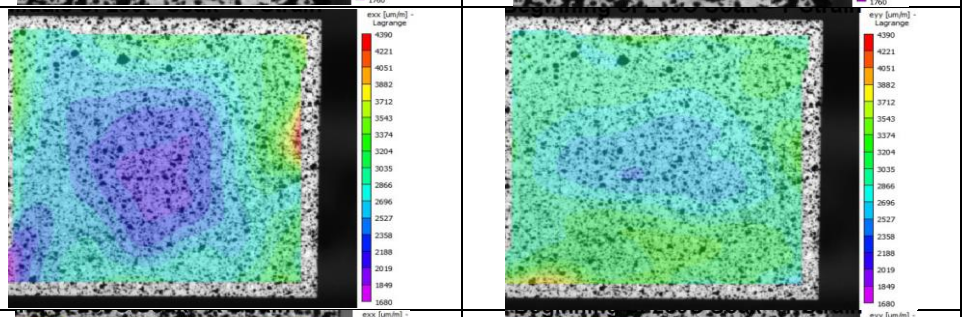
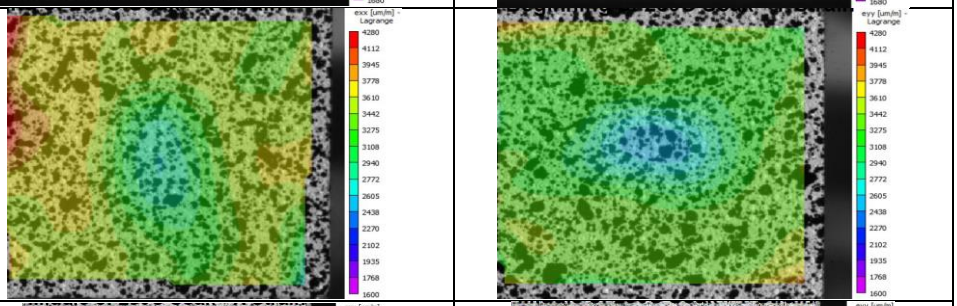
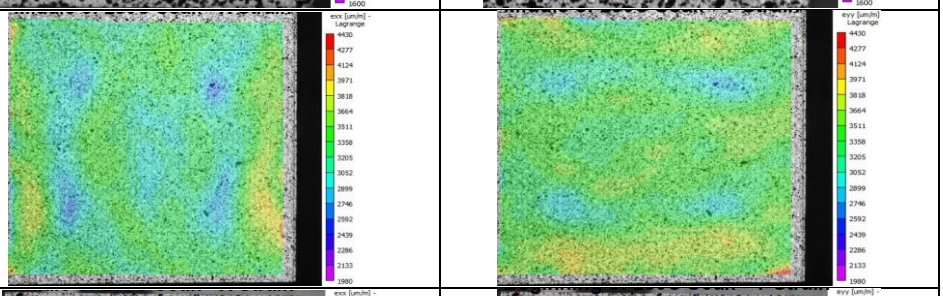
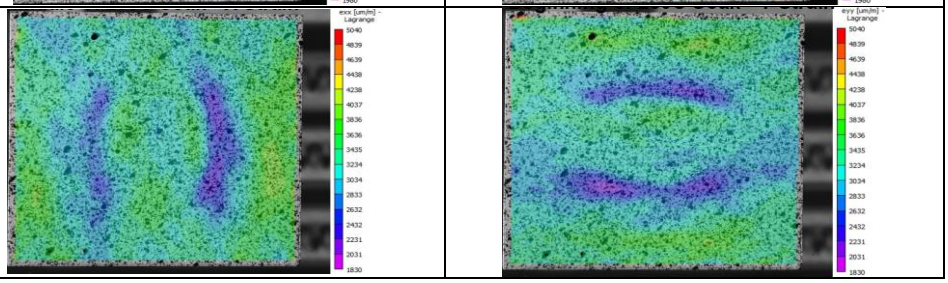
Pkg	x/y CTE (ppm/ºC)	Representative entire package x (left) and y (right) DIC images. Scales are in Microstrain.
A	11.9 / 12.4	
B	14.7 / 14.8	
C	13.6 / 14.6	
D	16.9 / 15.0	
E	15.9 / 16.2	
F	16.1 / 15.4	

Figure 13. Entire package bottomside x and y CTE values by DIC from room to 230ºC. Each CTE is the average of nine values (three samples times three measurements per sample). Representative entire package x and y DIC microstrain images.
*Originally published at SMTAI 2018

IN-PLANE PACKAGE CTE MEASUREMENTS

Digital Image Correlation (DIC) was used to measure the composite CTE of the package bottomside from room temperature up to 230ºC. Note that CTE measurements below room temperature were not currently possible. DIC is a non-contact, full-field optical technique that can measure both in-plane and out-of-plane displacements of an object's surface [8]. To prepare the sample, a high contrast, random speckle pattern was applied to the bottomside of all the packages. Three packages of each type were measured. To enable the measurement, two cameras are mounted above the sample in an oven, viewing the sample from different angles. The two simultaneous images from both cameras are then digitized. Using pattern recognition of the speckles within a small pixel window, the software identifies the same point on the surface from both perspectives. Using the principle of stereo triangulation, the spatial position of the pixel window relative to the cameras is determined in 3D space. Stepping the pixel window across the sample, the displacement of the surface can be mapped out in three axes. For the measurements performed in this study, in-plane strain measurement resolution was 100 microstrain.

Figure 13 lists the average CTE's across the entire package in both x and y for each of the sample types. Differences in the x and y values are generally caused by different substrate glass weaves in the two directions and the fact that most of the die were at least slightly rectangular. Also shown in this figure are representative images from the DIC system showing the resulting microstrain distribution across the entire part. The microstrain values shown for each pixel in the images were the result of averaging the microstrains over a 45 × 45 pixel area. The simple formula to convert strains to CTE is as follows, where ΔT is simply the 205ºC measurement range:

$$\text{CTE (in ppm/ºC)} = (\text{strain} \times 1{,}000{,}000) / \Delta T$$

Some of the lowest microstrains measured were in the center region of parts that were under the shadow of the die and were in the 1,600 to 1,800 microstrain range. Using the CTE formula above, this results in CTE's in the 8-9 ppm/ºC range. For the molded, large die parts which have thinner substrates, this lower CTE region extended outward considerably from the center of the package. For reference, silicon has a CTE of 2.6 ppm/ºC and SAC solder alloys are around 21 to 22 ppm/ºC, both at room temperature [10, 11]. All the package CTE measurements should be compared to that of the PCB the parts are soldered onto. The PCB's used for this study were comprised of epoxy-glass laminate with up to eight copper layers. Copper has a CTE of 16.7 ppm/ºC and the epoxy-glass laminate used for these studies was a multi-functional high Tg, low stress epoxy resin material with a CTE of 13-14 ppm/ºC.

CONCLUSIONS

Table 2 summarizes the observations for each part type after reviewing all the BLR solder joint failure locations in thermal cycling and correlating these failure locations to the in plane CTE and out of plane CoolMoiré warpage measurements. As can be concluded from the comments in the table, all the BLR BGA solder joint failure locations observed can generally be explained by the data.

Table 2. Summary of correlation of location of first solder joint failure in BLR to observations from both DIC in plane CTE measurements and CoolMoiré warpage measurements.

#	First Failure Location in BLR	Correlating Observations from CoolMoiré and DIC
A	Spheres in inner perimeter row just outside die corners	Lowest overall CTE of any package. Effect of the die is obvious with lower strain and therefore CTE all the way out to the edge of the die. Minimal out of plane warpage.
B	Spheres in exact center of the package / die	No die so relatively constant CTE across the entire package. Out of plane "discontinuity" in the center of the part at -40ºC believe to be caused by the presence of agglomerated die attach.
C	Spheres in inner perimeter row just outside die corners	2nd largest die to package ratio and 2nd lowest CTE. Similar to A, effect of the die is obvious with lower strain and therefore CTE in the center. Greater effect of the die in x direction since die is slightly rectangular.
D	Package corner spheres	Smallest die part. Die effect is only minimally visible. Out of plane package corner warpage, especially at -40ºC, explains corner BGA failures.
E	Sphere at the die corner inward from a depopulated row	In plane CTE effect of the die appears minimal. Out of plane warpage under the die is pronounced. Failures were at the edge of this region which also happens to be where there was a depopulated row. Refer back to Figure 1E.
F	Spheres in exact center of the package / die	Similar to E above except that out of plane magnitude is greater and there is no depopulated row. Center spheres are put in alternating tension/compression during BLR.

The following conclusions could be drawn from the current study which correlated BLR location of failure to package CTE and temperature dependent warpage behavior:

- Location of first failure in BLR was highly dependent on package attributes. Depending on the package, either the corner, center or under die edge spheres were observed to fail first. This failure location data can be used to, where possible, optimize pin assignments to maximize reliability in a given application. Package warpage and CTE measurements were successfully used to explain these first failure locations.
- For the type D part which had the lowest die to package ratio excluding the no die part, the silicon CTE mismatch effect was eclipsed by the overall package corner warpage which resulted in corner spheres failing first.

*Originally published at SMTAI 2018

- Surprisingly, a molded BGA assembled without any die was observed to have lower cycles to failure than with a die present by almost 3×. This was attributed to the localized warpage effect of the accumulated die attach on the center sphere area. Also of note is that this package with no die resulted in the lowest cycles to failure of any of the packages studied.
- The added stiffness from a bismuth containing SAC alloy increased the board-level characteristic life (eta) of one specific configuration, part type E, by over 3×. This package exhibited relatively low cycles to failure with the SnAg alloy primarily due to the location of a depopulated row right at the edge of the die.

ACKNOWLEDGEMENTS

The authors would like to thank Alvin Youngblood, Roy Arldt, Tom Battle and Arthur Green for their various contributions to this effort. Many thanks to Charly Olson at Akrometrix for taking the DIC CTE data. Also, thanks to George Leal, Franklin Utama, Andy Reinhart and Matt Zapico for extensive collaboration and for providing test vehicles used in this study. Lastly, thanks to Pascal Oberndorff and Tim Cheng for management support of these development activities.

REFERENCES

1) R. Darveaux, K. Banerji, A. Mawer, and G. Dody, "Reliability of Plastic Ball Grid Array Assembly," Ball Grid Array Technology, J. Lau Editor, McGraw-Hill, Inc., New York, NY, 1995.

2) A. Mawer and R. Darveaux, "Calculation of Thermal Cycling and Application Fatigue Life of Plastic Ball Grid Array (PBGA) Package," Proc. IEPS, 1993.

3) M. Petrucci, R. Johnson, A. Mawer, T. McQuiggin, B. Nelson and D. Rosckes, "Feasibility Study of Ball Grid Array Packaging", Proceedings, NEPCON East, Boston, MA, June 1993.

4) W. Loh, R. Kulterman, T. Purdie, H. Fu and M. Tsuriy, "Recent Trend of Package Warpage Characteristic", International Conference on Electronics Packaging (ICEP) 2015.

5) B. Zhao, V. Pai, C. Brahateeswaran, G. Hu, S. Chew, and N. Chin, "FEA Simulation and In-Situ Warpage Monitoring of Laminated Package Molded with Green EMC Using Shadow Moiré System", IEEE 7th International Conference on Electronic Packaging Technology, Shanghai, China. 2006.

6) T.S. Yeung, H. Sze, K. Tan, J. Sandhu, C.W. Neo and E. Law, "Enhancing WLBGA Board Level Reliability Through SACQ™, A New Lead-Free Solder Material", International Wafer Level Packaging Conference, 2014.

7) Y. Yang and P. Hassell, "Measurement of Thermal Deformation of BGA Using Phase-Shifting Shadow Moiré", Electronic/Numerical Mechanics in Electronic Packaging, pages 32-39, 1998.

8) J. Pan, R. Curry, N. Hubble and D. Zwemer, "Comparing Techniques for Temperature-Dependent Warpage Measurement." PLUS Produktion von Leiterplatten und Systemen, Oct. 2007.

9) N. Hubble, J. Young and K. Hartnett, "Surface Mount Signed Warpage Case Study; New Methods for Characterizing 3D Shapes Through Reflow Temperatures", Proceedings of IPC APEX, 2017.

10) R. Hull, "Properties of Crystalline Silicon", INSPEC, London, 1999.

11) T. Siewert, S. Liu, D. Smith and J. C. Madeni, "Database for Solder Properties with Emphasis on New Lead-Free Solders", NIST and Colorado School of Mines, https://www.msed.nist.gov/solder/NIST_LeadfreeSolder_v4.pdf , Release 4.0, February 11, 2002.

*Originally published at SMTAI 2018