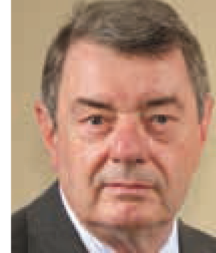

The Lead-Free "Whac-A-Mole"

Ron Leckie, President, INFRASTRUCTURE Advisors
Partner, Ackrell Capital, Board of Directors Member, Delphon Industries, LLC
Founding Member of the GlobalScot Network

LEADING-EDGE TECHNOLOGY is often like the favorite kids' game, "Whac-A-Mole", in that when one problem is solved, another often pops up in a different area. In our haste to solve one problem, we may have created another. One example we will discuss here is the drive over the last several years to convert to lead-free materials and manufacturing. While the motivation and pressures to expunge tin-lead solder are definitely well-intended and undoubtedly the right thing to do, they have worked with some other trends to exacerbate problems associated with substrate and board warpage.

Background

To put things in perspective, let's reflect back in time to consider the continuing evolution of electronics miniaturization. Silicon die were packaged for many years by bonding them base-down on a package lead-frame or substrate. Then electrical wire bond connections were made from the pads on the die surface to corresponding pads on the frame or substrate before being encapsulated with plastic or some form of sealed lid. The internal connections were in turn routed out of the package via metal leads, which the customer would then solder to printed circuit boards (PCBs). While the die needed to be in relatively flat contact with the package to be bonded and the package needed to be relatively flat to the PCB, there was more than sufficient flexibility in the wire bonds and package leads to take up any slack caused by non-flat surfaces, flexing or thermal expansion mismatch.

Driven over the past several years primarily by the needs of the hand-held electronics community, the die-to-package connection has been migrating more to flip-chip where the top surface of the chip or die is flipped face-down on the package base and metal bumps are directly soldered to the corresponding pads on the package substrate. Similarly, package-to-PCB connection has migrated to a direct (no-lead or lead-less) surface mount where flexible package leads are replaced by small solder balls or paste arrayed in a pattern across the base of the package – hence the term Ball Grid Array (BGA) package. These BGA packages are then mounted to corresponding patterns on PCBs by mounting them in position and reflowing the solder balls to make direct electrical connection between the chip's package and board. The resulting direct chip-to-package and direct package-to-board connections clearly now have much less flexibility to be able to withstand non-flatness or warpage in the surfaces that must come and stay together robustly for the end product to work. The continuing miniaturization of electronics has also driven chipmakers to drastically reduce the thickness (really thinness) of the silicon die and the thickness of the packages so that multiple die can be stacked in a single package (3D packaging) and multiple packages can be stacked on top of each other (POP, or Package-On-Package).

The Package-to-PCB Interface. *Image courtesy of Akrometrix*

Additionally, the electrical complexity has also been escalating due to Moore's Law, so to handle more and faster signals with more power in this smaller space, it requires the use of complex multi-layer laminates with metal patterns embedded within insulating materials such as resins. Of course, the various materials including silicon, metals and inorganic resins all have differing Coefficient of Thermal Expansion (CTE) so, when subjected to heat, this induces stress between the layers and can cause warpage. The direction and magnitude of the warpage is the result of complex variables including the number of metal layers in the board and their design layout.

While much of this is evolutionary and "business as normal" in the electron-

ics industry as we strive for increased functionality and performance in smaller form factors,

On top of all this, over the last decade the industry has had to convert, due to environmental concerns, to lead-free materials with lead-free solder being the operative one that has had the biggest impact on the electronics packaging trends described above. Lead-free solder requires higher temperatures than traditional tin-lead solder to become molten and reflow. This drives the need to change many of the materials that have been in use for decades in the manufacture of microelectronics components and systems. These new materials behave differently than their predecessors and, with the higher temperatures, exacerbate this warpage behavior. So, in solving the problem of removing lead, we now have increased the problems associated with warpage.

Manifestation

In terms of the final assembled product, this warpage can impact it by potentially causing some of the electrical joints between the semiconductor package and the PCB to either not make connection (a manufacturing yield and cost impact) or make a weak connection that works initially but fails over time/use (a reliability impact - and even greater cost impact).

The most common symptom of warpage has been coined, "HnP" or "Head in Pillow" which has been widely documented in the industry. This failure mechanism gets its name from the shape of the deformed solder joint which is created when the board and package warp in different directions to start separating as the solder joint forms through reflow. While there are other contributing factors such as misalignment, materials and thermal reflow profile, it is believed that warpage is a primary concern.

Figure 1 shows an example of package warpage changing over temperature from concave to convex. As the solder melts, the ball and paste are not in contact and reflow cannot occur before the solder surface starts to oxidize. On cool down the warpage reduces and the oxidized surfaces make contact but do not make a perfectly reflowed solder joint. In some cases, these will appear under visual inspection to have formed a joint but in actuality could be either resistive or even have no electrical contact. In either case, this represents a failure mechanism either at test or over time in the field. The transition to lead-free solder uses different materials and requires higher reflow temperature profiles which aggravate the warpage.

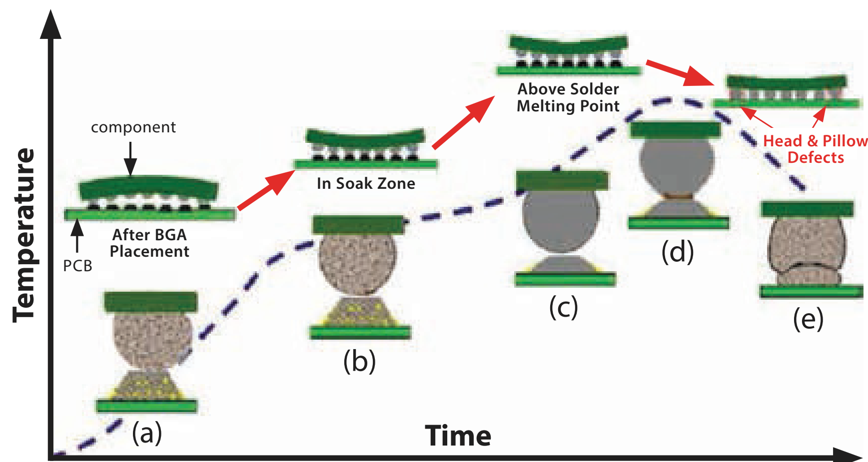

Figure 1. HnP Formation. *Image courtesy of Akrometrix*

Surfacing The Problem

As the market forces driving miniaturization resulted in increased interconnection challenges due to warpage, the EMS and ODM companies appeared to "keep the lid" on the problem by creatively tweaking the solder reflow process to accommodate the symptoms of warpage. This was achieved through such items as increased solder paste thickness or wider mask openings to deposit more solder selectively at weaker areas on circuit boards. This is what talented manufacturing engineers do – change processes to maximize yields and quality.

However, this warpage phenomenon was eventually surfaced as a problem by senior technologists at industry forums through technical papers on the topic. As voices became louder and it became apparent that this was a critical emerging industry problem, the various industry trade associations and standards bodies started working on it in pre-competitive forums. The result is that technology Roadmaps were developed to identify the problems and map out the need for improved flatness/warpage specifications and better design for manufacturability. As a result, standards have been developed and published to describe how to measure flatness/warpage on both components and printed circuit boards.

Standards

Momentum built across the microelectronics manufacturing community with papers on the problem being published by large companies such as Alcatel, Altera, Blackberry, Celestica, Delphi, Ericsson, Flextronics, Infineon, Intel, Micron, Sanmina, etc. The challenge in the fragmented supply chain was that without a common methodology to measure warpage, it was too easy to "point fingers" upstream or downstream while the failure mechanisms persisted. The initial challenge was in identifying standardized practical methods for measuring and quantifying warpage.

The resulting standards that have been published include JEITA's (Japan Electronics & IT Association) warpage specification; iNEMI's (International Electronics Manufacturing Initiative) Package Qualification Criteria and Roadmap; JEDEC's (formerly Joint Electron Device Engineering Council) standards that apply to measuring warpage for chip packages at temperature; and more recently, the IPC (originated as Institute for Printed Circuits) standard for board warpage. The process to obtain agreement on standards can be lengthy and difficult, but the fact that this recent IPC standard was developed in a year, and passed with approval on its first ballot, is a strong testament to the industry's support and commitment to finding solutions.

Solutions

With the right metrology in place to characterize a given application, it is then possible to make refinements

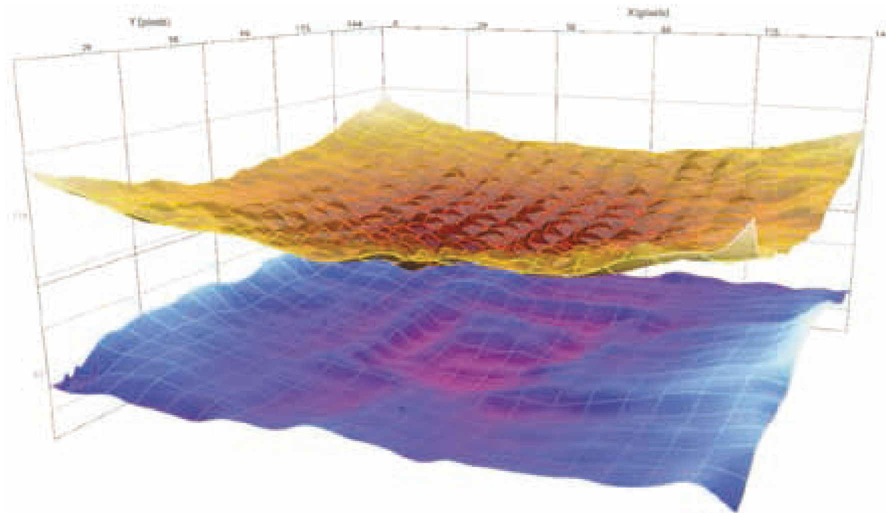

Figure 2. Package to PCB Interface Analysis. *Image courtesy of Akrometrix*

to the design, materials and process to minimize warpage and maximize quality and reliability of the interconnects. Traditional methods of measuring flatness include mechanical, optical and laser based methodologies. These are "static" methods that have not been shown to work in dynamic thermal environments where latent warpage shows up – in the solder reflow process.

In the late 1990's, technology and IP was developed at the Georgia Institute of Technology and has been licensed for commercialization to Akrometrix, based in Atlanta, Georgia. Their approach uses Moiré fringe techniques in a controlled environment for measuring dynamic temperature warpage. The output is an analysis of the dynamic movement of a single surface or between two surfaces showing high and low points of contact as they change across a selected range of temperatures. This approach has become so prevalent that its use is identified in the standards documents. Akrometrix designs, manufactures and sells various pieces of equipment that are used by package/substrate, semiconductor and printed circuit board manufacturers and subcontractors, as well as by OEMs (Original Equipment Manufacturers), EMS (Electronic Manufacturing Services) companies and ODMs (Original Design Manufacturers). They also provide contract lab services to characterize components and boards. Another company using similar techniques and providing both equipment and services is Insidix, based in France.

With characterization data and knowledge comes the ability to implement solutions. Software tools provide graphical and/or tabular reports and analysis of the surface warpage over temperature. A powerful capability is to analyze the potential fit of two mating surfaces, identifying likely problem areas when components come into contact with boards as shown in the example above (see Figure 2) from Akrometrix. Results may suggest a modification of design rules for substrates and boards to manage thermal coefficients of expansion and match their warpage characteristics. It may require selection of different materials, or changes to the solder mask, paste thickness, etc.

Conclusions

These approaches clearly indicate that warpage and HnP type of defects must be addressed up-front at the design and development phase. There is no practical production screen available for dynamic thermal warpage, so the product, package and process combinations must be thoroughly characterized up-front before entering into a controlled high-volume manufacturing process. It may have taken the industry time to own up to the fact that in switching to lead-free it had created or at least aggravated warpage problems and the resulting contact failure mechanisms. However, it would appear that methods and solutions are available to help quantify and resolve the issues.

This is surely a case of an "ounce of prevention" being worth "a pound of cure." ◆

About the Author

Ron provides consultation services to clients in the areas of strategic marketing, business development, market & technology diligence, merger & acquisition, and expert witness services. Prior to starting his consulting practice in 1995, Ron enjoyed 25 years developing his expertise in the semiconductor manufacturing industry with specialties in product, packaging and test technology. This included 14 years of engineering and manufacturing within the semiconductor industry and 11 years of system-level development and marketing in the capital equipment industry. During his career in the semiconductor industry at Signetics/Philips, Ron managed the functions of semiconductor yield management, product & test engineering, quality management and operations. In the capital equipment industry, he gained his marketing skills, managed a product P&L center to develop and bring new system-level products to market, and was a member of the executive staff at Megatest Corporation, taking the company through a successful turnaround and IPO.

Ron has published numerous articles and papers, and has participated in many panel discussions on the business and technical aspects of the industry. In 2005, he researched and wrote "Funding The Future", an in-depth white paper identifying the $9 billion R&D funding gap facing the semiconductor supply industry by 2010 to maintain the "Moore's Law" pace defined within the International Technology Roadmap for Semiconductors.

Ron earned his Bachelor of Science degree with Honours in Electrical & Electronic Engineering in 1970 from Heriot Watt University, Edinburgh, Scotland.

In addition to being President of INFRASTRUCTURE Advisors, Ron is a partner at Ackrell Capital and a member of the Board of Directors of Delphon Industries, LLC. He is a very active volunteer on several SEMI committees and is a founding member of the GlobalScot network.