UNDERSTANDING PCB DESIGN VARIABLES THAT CONTRIBUTE TO WARPAGE DURING MODULE-CARRIER ATTACHMENT

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ABSTRACT
PCB warpage has been identified as a possible contributor to unacceptable yield rates during reflow assembly of a module to a carrier board. The module has a land grid array pattern and is placed directly on solder paste on the carrier board. This results in low-profile solder joints which are sensitive to the coplanarity of both the module and the carrier boards. The typical failure mode is one or more solder joint opens caused by a lifted corner of the module after reflow.

In an effort to improve attachment yield rates, a design of experiment has been proposed to evaluate several PCB design variables that are believed to contribute to warpage during reflow, including: (1) laminate material, (2) layer-to-layer copper balance, (3) panel configuration of the 6-up module array and (4) location of the 6-up array in the PCB fabricator's working panel. To simplify the investigation, only the variables associated with module PCBs are considered; the carrier PCB design is held constant.

Shadow Moiré technique will be used to provide accurate warpage profiles of the 6-up module arrays before and after top- and bottom-side assembly, and again before and after attachment to the carrier board. A large volume of samples will be tested in order to gain statistical relevance of the data and correlate any yield problems to initial warp. The objective is to isolate the key design parameter(s) that contribute most to attachment problems.

Key words: Warpage, Land Grid Array, Copper Balance, Shadow Moiré

INTRODUCTION
The subject of this paper is a WiFi module is soldered to one of several different product-specific carrier PCBs. The module is an 8-layer ELIC PCB, 30x40mm and 0.77mm thick, fabricated with a mid-Tg, halogen-free laminate. The module has an LGA pattern with 333 pads 0.6mm square and ENIG surface finish. There are several configurations of carrier boards, but all are 1.57 mm thick with immersion silver finish. Figure 1 shows (A) the LGA pattern of the module, (B) the corresponding pattern on a representative carrier board and (C) the assembled module-carrier system.
Shortly after product launch, solder opens between module and carrier interconnect were detected at ICT. Assemblies were failing at a 50,000 ppm defect rate. Prying the module off the defective assembly reveled that there had been no solder contact between the module PCB and the paste on the carrier pads on the lifted corner of the module, as shown in Figure 2.

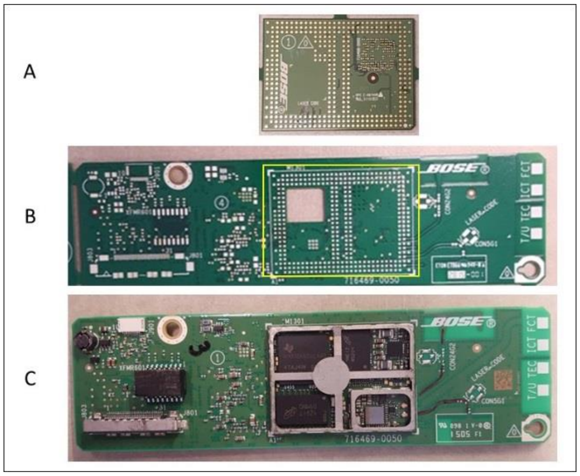

Figure 1. (A) WiFi Module LGA pattern, (B) corresponding LGA pattern on a representative carrier board and (C) assembled module-carrier system

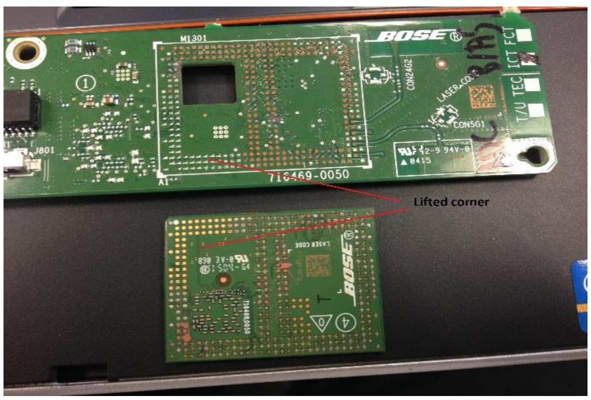

Figure 2. A failed module-carrier assembly after separation showing no solder on the pads in the lifted corner of the module.

ASSEMBLY PROCESS

The module is assembled in a conventional SMT processes building bottom sides first, followed by top side assembly. The Module and Carrier boards are SMT only designs with no Thru Hole components. The module was panelized in a 6 up array and the carrier in a four up. Several of the critical components on the module were type 3 MSD devices with an exposure limit of 168 hours. Since the module would be soldered to the carrier as an SMT device it is critical that it be handled as an MSD once assembled. To avoid baking the exposure times are tracked during subsequent test processes and are stored in dry boxes. Once tested the module is routed and placed into JEDEC matrix trays with desiccant packaging and place in stock till needed for assembly to the mother board.

It was recognized in early prototypes that maintaining PCB flatness during the process would be an important factor for successful soldering of the Module to the carrier. This led to a decision to use process carriers for both the module and carrier. Figure 3 shows a typical SMT process carrier. For the thinner module the pallet would be a significant process enhancement providing Solid board support for printing and placement. For the carrier the pallet was primarily to control the board sag common during the double sided reflow process.

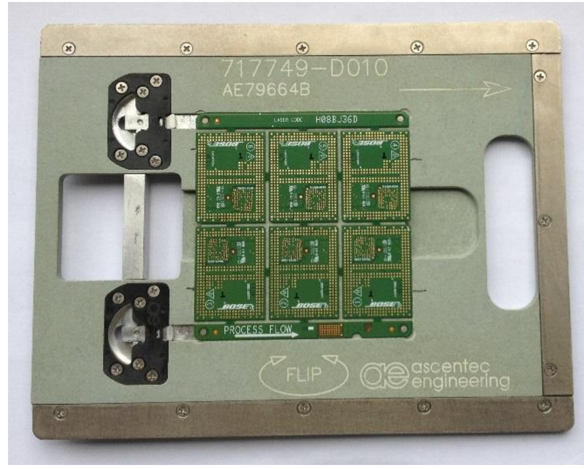

Figure 3. Module Panel in Process Pallet

FISHBONE ANALYSIS

A team was formed consisting of the Plant Supplier and Process Quality, Plant Process Engineers, Corporate Manufacturing Engineers, Design Engineers and PC Board Commodity Engineer to analyze the problem following a DIMAIC methodology. A key part of that process is to develop a cause and effect diagram outlining the process to identify potential areas having an influence on the defect as shown in Figure 4 below.

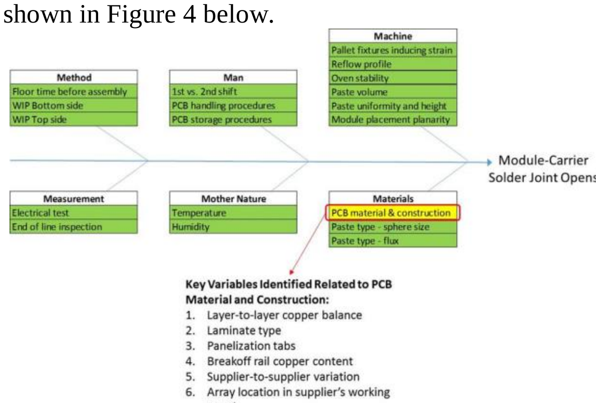

Figure 4. Cause and Effect Diagram

The team evaluated each item in the diagram, performing process audits for MSD processes and work methods, analyzing data for environmental control and analysis of process parameters. The oven profiles were checked to the paste supplier's recommendation and no variations were found. The modules were thermo-coupled in the four corner and center during the carrier assembly process and were found to be within 1.5°C across the part.

When the module panels were checked for flatness using the methodology in IPC-610 [1] the modules were found to be within the 2mm allowed for a panel this size. For the module this would translate to a .75mm warp. It became clear that the IPC would be fine for assembly of regular PCB it was not tight enough to solder an LGA into 7 mils of solder paste. Considering that to specifications for BGA packages would be more applicable the JEITA specification on BGA package warpage [2] was referenced. The spec for FLGA packages was found to roughly fit our module. Our pitch 1.27mm was larger than the .8mm maximum pitch in the table but, the trend for all the devices was that the maximum warpage could not exceed the height of the molten solder on the component site. Realizing that this speciation would be too tight for the PCBs on hand and would adversely affect the material the team decided to use the .177mm (.007") paste height as the standard. A jig was developed to hold the modules and they were to be inspected using a go/no go shim before packaging into trays. While evaluating the raw panels it was observed that approximately 10% of those received were severely warped. In order to increase yields of finished modules and avoid scrap a sorting process was developed for the raw panels. Panels would be sorted into 3 categories, A<.5mm, B >.5mm, <1mm and C >1mm. Only group A PCBs would be built. With these controls in place the defect rate for unsoldered modules dropped ranging from lows of 2,000 to 10,000ppm.

With a containment in place the team began working on areas of the fishbone to discount non-contributing factors, improve board flatness and adjust process variables to improve yields. Baking boards did not improve flatness. Boards baked with weights to flatten the panels improved them to acceptable levels but they relaxed to their original condition over several days. Increasing solder paste height and volume did not significantly improve the process and began to produce shorts. Profile adjustment had no effect. Several samples of the module and carrier were sent out for Shadow Moiré analysis. The evaluation determined that the PCBS were changing during the reflow processing with the module warping upward (smiling) and the carrier warping downward (frowning). It became clear that the board stability needed to be improved. The team met with technical resources from the two board suppliers and discussed PCB variables which could affect flatness. The major potential contributors identified were the material selection and copper balance. Less impact was expected from process changes at the supplier. Those changes included baking under pressure and better flatness sorting techniques. While the suppliers developed proposals for different materials the design team investigated changes to copper balance and the panel design. Figure 5 show the existing and proposed copper balance.

	Existing	Modified
Pri	40.00%	61.40%
In2	87.10%	87.10%
In3	67.70%	67.70%
In4	65.60%	65.60%
In5	88.50%	88.50%
In6	58.30%	58.30%
In7	82.80%	82.80%
Sec	80.30%	63.10%

Actual Copper change

No changes made to the CU on inner layers.

Figure 5. PCB Copper Balance

One observation was that while the module copper had etches and reliefs the rails had unbroken planes. This is commonly done to stiffen panels and prevent sag in the reflow process. The team questioned whether it might impart stress during heating or in the lamination process. Another observation was that the corners where the defects occur were not tied in to the panel. Breaks had been placed in the center to minimize tabs and reduce routing time.

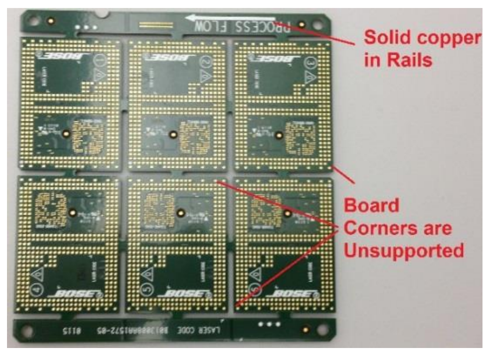

Figure 6. Module Rails and Break Tabs

The final attribute the team felt might be significant was fabricators working panel position. The assumption was that modules from the corners of the working panel would have a greater warp than those from the internal portions of the sheet.

EXPERIMENT DESIGN

Upon completing the cause and effect analysis the team began to design and experiment to answer the two main questions coming out of the evaluations. First, was variation in the process causing defects or was PCB flatness the defining factor. Despite the experiments and evaluations done the measurement capability limitations left this question unanswered. The process was demonstrated to be in control and followed convention in regards to printing placement and reflow parameters. The second question focused on the raw PCBs. Which changes made to the materials and designs would have the greatest impact to the PCB flatness.

Phase one of the experiment would measure the full population of PCBS in groups A, B and C at each process step to determine whether the boards were changing as they were processed and by how much. Working with our statistical engineer the board quantities needed for a valid experiment were determined and a matrix designed. Panels from each of the A B and C groups would be run to verify whether the starting board warpage was the leading factor in solder opens or if the process had a significant impact. Table 1 shows the PCB Sample quantities.

Table 1. Phase 1 Sample Allocation

Phase 1

Sample Allocation (by individual circuit and 6-up panel)

	Modules		Panels (6-up)	
Group	Supplier A	Supplier B	Supplier A	Supplier B
A Warp <0.5mm	1380	1380	230	230
B Warp >0.5mm, ≤1mm	1380	1380	230	230
C >1.0mm	438	726	73	121
TOTALS	3198	3486	533	581

Phase two of the experiment would involve the same measurement strategy as phase one using PWBs implementing the material and design changes the team wished to investigate. Attributes to be studied were the materials, panel position, copper content of the rails, board break quantity and position and the copper balance. Each supplier had a different recommendation on material. Supplier A recommended a BT core with the existing material used for the cap layers. Supplier B recommended a different laminate they felt was more stable. Table 2 shows the PCB quantities by attribute and supplier.

Table 2. Phase 2 Sample Allocation.

Phase 2

Sample Allocation (by 6-up panel)

Sum of Total # arrays in group	Column Labels						
	Supplier A		Supplier A Total	Supplier B		Supplier B Total	Grand Total
Row Labels	Existing Material	Existing Material/ BT Hybrid		Existing Material	Alternate Material		
1 - Control - non-corner	55	55	110	24	24	48	158
2 - Control - corner	20	20	40	24	24	48	88
3 - Breakoff Rails	25	25	50	24	24	48	98
4 - Cu etch	25	25	50	24	24	48	98
5 - Extra routing tabs	25	25	50	24	24	48	98
Grand Total	150	150	300	120	120	240	540

With the build matrix designed it was found that cost for multiple variations of the PCB would add significantly to the budget of the experiment. In an effort to reduce the fabricators set ups and individual types required the variations were combined into a single working panel with different panel locations having different attributes. The new material variations and the existing material controls would be built using the same working panel designs. Each supplier had its own working panel size so a separate but similar layout was made for each. Each supplier used a different working panel size so a separate but similar matrix was designed for each. Figure 7 shows one of the suppliers working panels. Table 3 shows the key to the variations in the working panel.

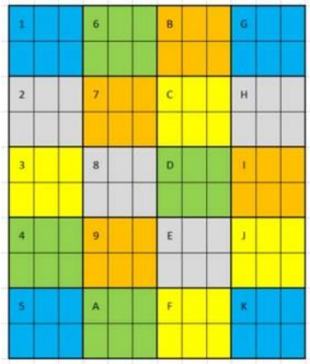

Figure 7. Working panel for suppler 1

Table 3. Working Panel Variant Key

Group Color ID	Sample description	Working Panel Locations	# of Bose arrays for each location	Total # arrays in group	Total # boards in group
Grey	Original artwork: non-corner location	2, 8, E, H	6	24	144
Blue	Original artwork: corner location	1, 5, G, K	6	24	144
Green	Modified artwork: reduced Cu in Bose breakoff rails	4, 6, A, D	6	24	144
Yellow	Modified artwork: extra panelization tabs	3, C, F, J	6	24	144
Orange	Modified artwork: balanced Cu etch	7, 9, B, I	6	24	144
			Totals	120	720

MEASUREMENT NEEDS AND METHOD SELECTION

While designing the experiment the team became concerned with the large number of measurements needed. With plans to measure 1654 module panels 3 times and 2481 carrier panels resources would become a problem. Splitting the measurements into individual boards would yield 39696 pieces of data for analysis. Table 4 illustrates the labor hours for three automated measuring strategies. Selecting the correct measuring method would be critical for success. The quantity of modified PCBs for the phase 2 portion of the experiment were limited to one run leaving no opportunity to recover from mistakes or corrupt data. The team looked a numerous ways to collect data and found each with this drawbacks. Automated methods would be costly in equipment and technicians but, manual method would costly in speed and accuracy. The following paragraphs describe the advantages and disadvantages of each option considered.

Measurment Times

	Laser CMM	Laser Sensor	Shadow Morié
Total # of Module Arrays to Measure	1654	1655	1654
Measure3 X Raw, BSS, TSS Mods	4962	4965	4962
Measure TSS Carriers (4 up)	2481	2482	2481
Total panels measurements	**7443**	**7447**	**7443**
Time to measure each (Sec)	210	60	35
Total Time Required (Hours)	**434**	**124**	**72**

Table 4. Measurement Time Comparison

Use Only Test Pass/Fail Data. This method would not measure boards at all, but use only the A, B and C classifications for phase one and the attribute changes groups for phase 2. While fast and low cost this was deemed unacceptable. This method would produce no process insight and given the low defect rates there would not be enough information to identify trends and draw any meaningful conclusions.

Hand Measuring With Pins And Gauges. This was the method currently in use. This could be implemented quickly but the measurement was slow and the results subject to the variability of the operators. The precision would also be low. It was decided that this method would not produce the information needed for sound conclusions.

In House Laser CMM. Measuring would be done using a system located in the corporate R&D center. This method would produce the quality of data needed for success and used existing resources. The disadvantage of this method were the long measuring time of our system (3.5 minutes), the lab hours required (400 hrs) which would be charged to the project and the logistics of shipping boards between corporate on the east and the plant on west coast. These factors combined to make this an undesirable option. It was also considered that long stretches between measurement and further processing could make the information unrepresentative of the existing process where boards are completed in two to three days.

Use A Metrology Contractor Near The Plant. To counter the logistics issues of shipping boards to the corporate lab the team searched for a metrology lab with similar capabilities local to the plant. It was assumed the cost and measuring time would be similar which would still be a disadvantage. No suppliers were identified for this volume of measurement so this option was discounted.

Purchase A Laser CMM For The Plant. This option would mitigate the disadvantages of using the corporate lab equipment and would provide and additional capability locally to production. Plant labor could be used at a lower rate and additional shifts are available to get measurements done within the schedule. The disadvantages of this option are the cost of the equipment ($85K-$90K), the lead time and training to set up the equipment and the justification and approval cycle required for capital equipment. The lead time and cost of this method eliminated it from consideration.

Develop An In House Measurement System. The team identified a line scan laser sensor which could quickly take precise measurements. The supplier also offered a data analysis software. With an in house equipment design group and a precision gantry work station available this seemed like a low cost alternative which could be implemented quickly using existing resources. The equipment group estimated a cycle time under one minute which was an improvement over the Laser CMM in the lab. This system would enable co-location of the equipment on the production floor. Measurements would be taken between board sides within the cycle time of the SMT process, thus ensuring that the measurements take were representative of the process as it is run on a daily basis. After working with the sensor and its software it was found that the program development time was far more than initially thought. Engineering labor costs were estimated at $18,000. With the purchase of the sensor the project would cost over $28K. Being a development project it was likely there would be bugs at the startup of the equipment. This presented a significant risk to the project if the data was corrupted or lost. This alternative was put on hold to investigate several of the other options described above.

Lease A Shadow Moiré. Having run an evaluation during our investigation of likely defect causes the team had become familiar with its capabilities and had maintained a relationship with the manufacturer's representative. While discussing further testing it was suggested that leasing the Shadow Moiré might be a viable option for the project. The equipment could be used without the heater for a quick cycle time. With a measurement time of less than 2 seconds, and data density of ~250 microns per data point, a large, dense amount of data could be captured to fully characterize the surface shape of the modules' and carrier boards' interconnect area. The equipment would also collect the entire board topology where many of the previous options were point-to-point, or scanning techniques which have significant tradeoffs between data density and measurement time. The equipment was a fully developed production system with user software tools for data analysis further reducing risk and analysis time. The supplier would provide on floor training and support for the start up. While the costs were similar to the in house development project the risk was far lower and the capability significantly greater. Given its advantages in many areas and the technical support available leasing the Shadow Marie was chosen as the best option for this project

Shadow Moiré Overview

Shadow Moiré is a non-contact, full-field optical technique that uses geometric interference between a reference grating and its shadow on a sample to measure relative vertical displacement at each pixel position in the resulting image. Figure 8 provides a visual diagram of the process. It requires a Ronchi-ruled grating, a white line light source at approximately 45 degrees to the grating and a camera perpendicular to the grating. Its optical configuration integrated with the heating chamber is shown in the Figure 8 below. A technique, known as phase stepping, is applied to shadow moiré to increase measurement resolution and provide automatic ordering of the interference fringes. This technique is implemented by vertically translating the sample relative to the grating.

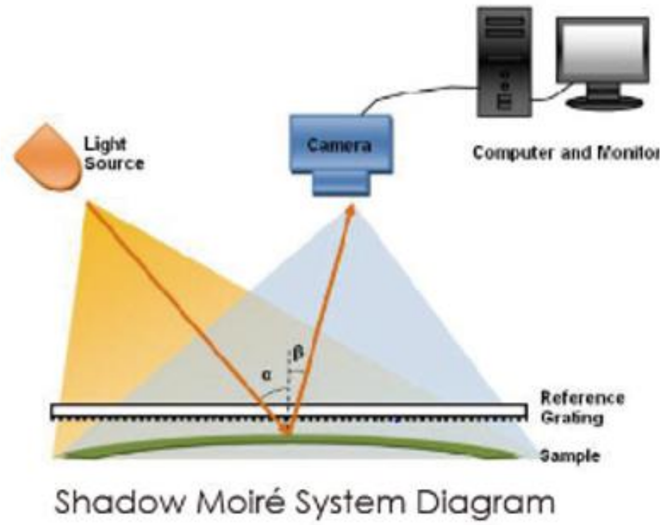

Figure 8. Shadow Moiré Process Visual

As discussed above, shadow moiré offered several distinct advantages as compared to the other measurement methods considered. With a measurement time of less than 2 seconds, and data density of ~250 microns per data point, a large, dense amount of data could be captured to fully characterize the surface shape of the modules' and carrier boards. In addition to the interconnect area coplanarity value, it was thought that measuring the module-board height after final assembly would also be a useful data point. This was not possible, however, as shadow moiré has a maximum step height measurement capability of ~50-100 microns.

Although typically used for at-temperature characterization of parts/assemblies, the tool could be adapted to measure the thousands of parts needed for this study. After some fixture modifications and operator training, a scan time of roughly 35 seconds per panel was achieved. This process involved some overhead that would not be needed in a more simplified, room-temperature only, tool. The parts were tracked via serial number for later correlation. Data for the entire panel was taken all at once and partitioned into smaller regions in post-processing. A workflow diagram of the measurement process is shown in Figure 9 below.

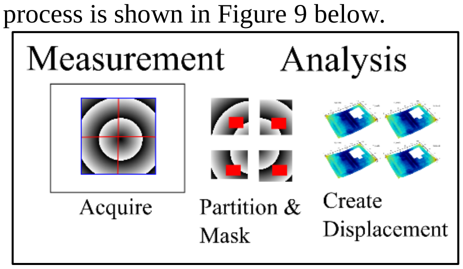

Figure 9. Data Processsing Steps

RESULTS

Phase 1

The purpose of Phase 1 was to determine whether the PCB flatness was the most likely root cause in solder opens at the carrier assembly. Only 5 of the 6 A, B and C groups could be built. Supplier 2 had recently been discontinued as a supplier leaving no Group A from them in stock. The modules were all 2D laser bar coded and measured in the Shadow Moiré before use. They were then measured again after bottom and top side SMT assembly. All the measurements were collected at the panel level and the data then processed to crop it into individual modules. An automated coplanarity analysis was then run and histograms created for each group. The plots in Figure 10 and 11 below show the coplanarity distribution in microns on the X axis and the percentage of modules at each measurement on the Y. With the data broken down into individual boards measurements were not as concentrated as expected. Each group had a similar distribution of boards in the higher ranges regardless of its level in the hand sorting process. After processing the coplanarity had shifted 60 microns higher with no measurements in the lower than 90 microns. The percentage of measurements in the lower warpage region also shrunk from 25-35% in the unprocessed boards to 15-20% after processing.

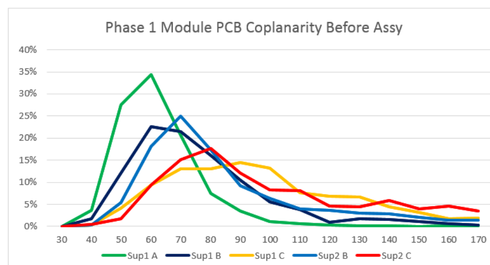

Figure 10. Unprocessed Module Measurement Distribution

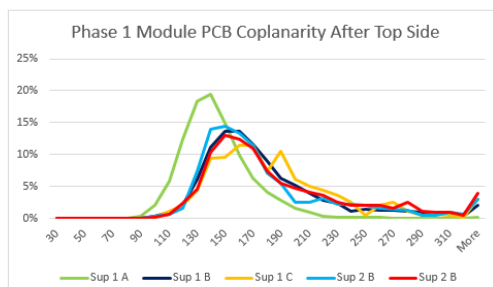

Figure 11. Post Top Side Module Measurement Distribution

With the process data showing the boards changing during the processes it was decided to run an additional analysis of boards at processing temperatures using Shadow Moiré. A module and carrier panel were sent to the equipment supplier and characterized at temperature to analyze thermal warpage effects that can impact solder joint formation. Warpage values vs temperature were graphed and gap values between the two surfaces was also analyzed. This gives an idea of how the two parts are moving relative to one another in the reflow oven.

Given that the paste thickness was roughly 165 microns, and this collapsed to roughly half that height at liquidus, a gap fail and warning map was created at 82 microns and 50 microns, respectively. After analyzing the 4-up carrier panel and 6-up module panel, statistical surfaces representing the part behavior at eleven temperature points were created. Figures 12 and 13 below show the average and maximum case at peak temperature respectively. Gap failures were noted prominently in one corner, and correlate well with open failures seen in production.

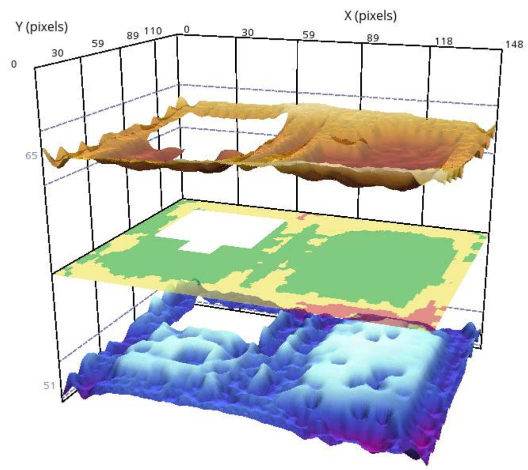

Figure 32 Average Plot at Peak Reflow Temperature

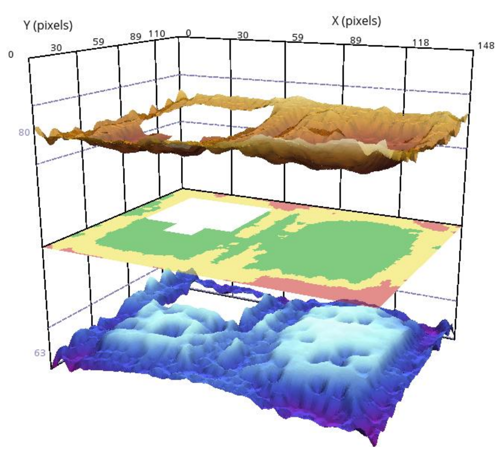

Figure 13. Maximum Plot at Peak Reflow Temperature

Gap vs. Temperature plots condensed the surface plots above into a broader picture of the assembly gap behavior over temperature. Three cases were analyzed, the maximum gap across the sample surface, the average gap, and the 3 sigma gap (average gap plus 3 standard deviations based on the gap distribution). In addition, 2 different statistical surfaces were analyzed, average and maximum. These surfaces represent the average of the input surfaces and maximum of the input surfaces, respectively. In this case, there were 4 real bottom surfaces from the carrier panel, and 5 real top surfaces from the module panel that made up these statistical surfaces. Looking at the Gap vs. Temperature plots below in Figures 14 thru 16, the fact that the maximum gap and 3 sigma gaps were so similar in both plots indicates that the surface shape distributions were very close from part to part. Indeed, looking at the individual surface signed warpage values in Figures 14 thru 16 below shows that the samples were typically within 10-15 microns of one another. Based upon these two panel's behavior at temperature, and the typical paste height described previously, it could be assumed that the maximum gap values typically exceed this paste height at peak reflow temperatures. Of course this ignores the paste's surface tension and elasticity, but with less well behaved input carrier/module surfaces, the gap values could get quite large.

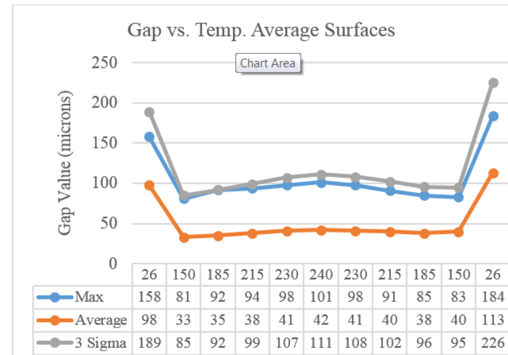

Figure 14. Average Gap vs Temperature

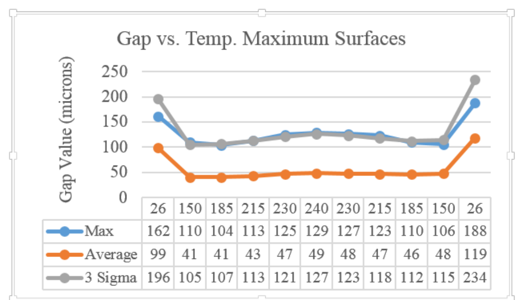

Figure 15. Maximum Gap vs Temperature

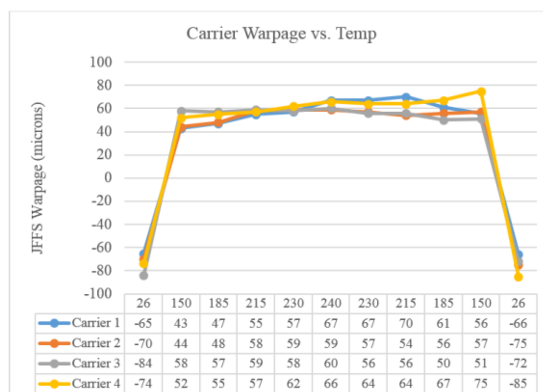

Figure 16. Carrier Warp vs Temperature

While it was clear the boards were warping further during processing the relationship that coplanarity had a significant impact on failures in production still needed to be confirmed**.** The actual ICT test failure rate by board suppliers and groupings were compared and are shown in Table 5. The failure rate of Group A boards from panels measuring under .5mm were very good at 513PPM. As the initial warpage increased in groups B and C the PPM levels increased significantly indicating that incoming panel flatness did have an effect on the process yields.

Table 5. Test failure Rates by Group

Phase 1 Defect Rate by Group

Group	PPM
Supplier 1 A	513
Supplier 1 B	24691
Supplier 1 C	45045
Supplier 2 B	23810
Supplier 2 C	55556

To anlayse whether there was a difference between suppliers or position in the module panel contingency tables were created to compare these attributes. These are shown in Table 6. The supplier table initally indicated that the supplier was a factor but, further anlysis of the data show that the absence of supplier 2 Group A boards underrepresented supplier 2 so that analysis was not used. The team had originally theorized that the corner boards of the module panel would be the least flat. Analysis of the board position revealed that there was no relationship (P-value>0.05) to individual module position in the panel and the likelyhood of failure.

Table 6. Analysis of Board Position in Panel

Board Position Contingency Table

		Pass	Fail	Total
Board 1	Row count	785	16	801
	Row percent	98	2	100
Board 2	Row count	785	16	801
	Row percent	98	2	100
Board 3	Row count	789	12	801
	Row percent	98.5	1.5	100
Board 4	Row count	784	17	801
	Row percent	97.88	2.12	100
Board 5	Row count	790	11	801
	Row percent	98.63	1.37	100
Board 6	Row count	784	17	801
	Row percent	97.88	2.12	100
Total	Row count	4717	89	4806
	Row percent	98.15	1.85	100

Pearson Chi-Square = 2.393, DF = 5, P-Value = 0.793

Likelihood Ratio Chi-Square = 2.496, DF = 5, P-Value = 0.777

Comparing the coplanarity averages of the failed modules with those of passing modules there was a difference between them as illustrated in the graph and table in Figure 17 below.

Coplanarity after TSS

	Sample size	Average (mm)	Std. Dev. (mm)	Minimum (mm)	Maximum (mm)	Statistical comparison of averages (averages with the same letter are statisticaly the same)
Fail	89	0.28593	0.0881	0.124	0.512	A
Pass	4717	0.15996	0.0437	0.084	0.57	B

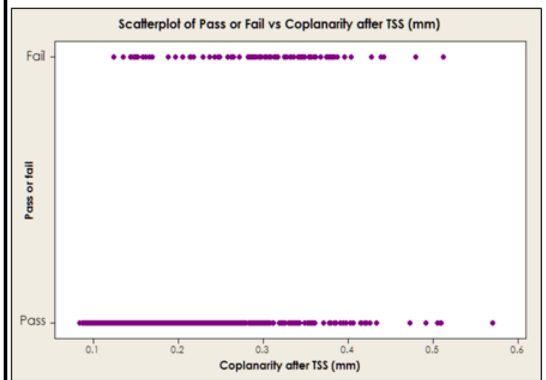

Figure 17. Defect Relationship to Coplanarity

Running a Logistic Regression Analysis to determine the likelihood of defects at a given flatness revealed the defect rate could be predicted and that there was a relationship between flatness and board opens at carrier assembly. The graph in Figure 18 shows that at .177mm coplanarity there is a 1.08% chance of a solder open defect. This correlates closely with the production yields of 1% less defects.

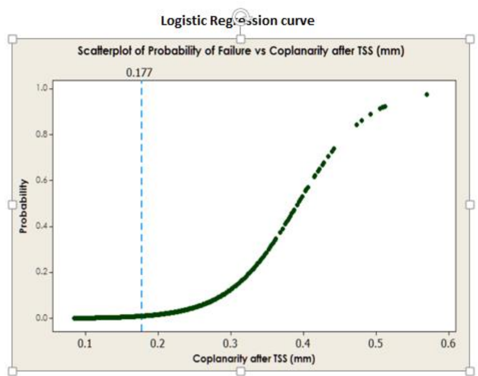

Figure 18. Failure Probability Curve

Phase 2

Phase 2 of the experiment was designed to evaluate changes in the design and materials for improved PCB flatness and stability in the process. PCBs were not sorted into flatness groups as was done in phase one and instead all boards from the process were used as received. There were 20 groups planned for analysis with variations of the materials and design changes. Table 7 describes the attribute groups with the changes and materials used for each. Groups E and J from supplier 2 were not received in time and left out of the evaluation.

Table 6. Analysis of Board Position in Panel

Supplier	Material	Group	Attribute
Supplier 2	Existing Material	A	Control Working Panels Non Corner
Supplier 2	Existing Material	B	Control Working Panels Corner
Supplier 2	Existing Material	C	Reduced copper density in the rails
Supplier 2	Existing Material	D	With extra routing tabs moved to corners
Supplier 2	Alternate Material	F	Control Working Panels Non Corner
Supplier 2	Alternate Material	G	Control Working Panels Corner
Supplier 2	Alternate Material	H	Reduced copper density in the rails
Supplier 2	Alternate Material	I	With extra routing tabs moved to corners
Supplier 1	Existing Material	K	Control Working Panels Non Corner
Supplier 1	Existing Material	L	Control Working Panels Corner
Supplier 1	Existing Material	M	Reduced copper density in the rails
Supplier 1	Existing Material	N	With extra routing tabs moved to corners
Supplier 1	Existing Material	O	With Balanced Copper
Supplier 1	Hybrid	P	Control Working Panels Non Corner
Supplier 1	Hybrid	Q	Control Working Panels Corner
Supplier 1	Hybrid	R	Reduced copper density in the rails
Supplier 1	Hybrid	S	With extra routing tabs moved to corners
Supplier 1	Hybrid	T	Balanced Copper
Not Received			
Supplier 2	Existing Material	E	Balanced Copper
Supplier 2	Alternate Material	J	Balanced Copper

The analysis was begun by comparing the coplanarity of each variation and looking for the best flatness and least variation. Looking at the raw board data there were clear indications that one variation might be better than the others. Once the data for processed boards was analyzed the leading candidates changed. This occurred after both bottom side and top side assembly. The results of the analysis after top side are shown in Table 8 and graphed in Figure 19. After top side processing groups K, N and O showed the best resulting average coplanarity. These variations were all from supplier one, used the existing material. Group K was from a working panel non corner, Group N had the additional board breaks at the corners and Group O had balanced copper top and bottom.

Table 8. Post Top Side coplanarity Measurements

Experimental group ID	Sample size	Average (mm)	Std. Dev. (mm)	Minimum (mm)	Maximum (mm)	Statistical comparison of averages (averages with the same letter are statisticaly the same)
G	126	0.18521	0.04169	0.107	0.377	A
R	150	0.17858	0.01971	0.141	0.272	A B
B	162	0.16978	0.02435	0.122	0.27	B C
F	198	0.16952	0.02185	0.117	0.283	B C
H	222	0.16729	0.01843	0.101	0.237	C D
I	162	0.16709	0.01641	0.135	0.225	C D
D	144	0.16681	0.01932	0.124	0.253	C D
M	150	0.16179	0.0293	0.114	0.37	C D E
A	216	0.15954	0.01855	0.107	0.263	D E
C	198	0.15665	0.02128	0.107	0.257	E F
P	330	0.15061	0.01876	0.097	0.302	F G
T	150	0.14999	0.01627	0.099	0.2	F G
S	150	0.14711	0.01503	0.109	0.188	G H
Q	120	0.14579	0.03695	0.087	0.336	G H
L	120	0.14574	0.04084	0.085	0.282	G H
O	150	0.13748	0.02493	0.076	0.217	H I
K	330	0.13364	0.0302	0.084	0.277	I
N	150	0.13341	0.02881	0.084	0.293	I

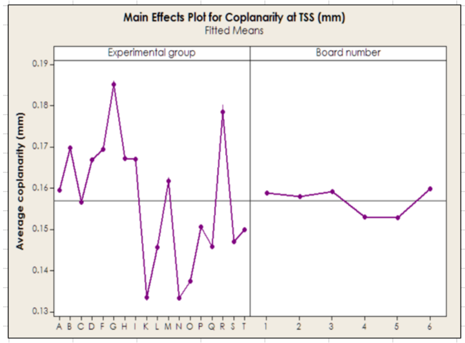

Figure 19. Plot of Average Flatness by Group

Looking at a plot of the coplanarity averages for passing and failing boards revealed that the passing boards had a smaller average and standard deviation but also had a significant number of points outside the box as shown in Figure 20 below. This would make it difficult to point to a specific coplanarity as needed to produce a passing result.

Pass or fail	Sample size	Average (mm)	Std. Dev. (mm)	Minimum (mm)	Maximum (mm)
Fail	36	0.2042	0.074	0.096	0.377
Pass	3192	0.15533	0.02734	0.076	0.37

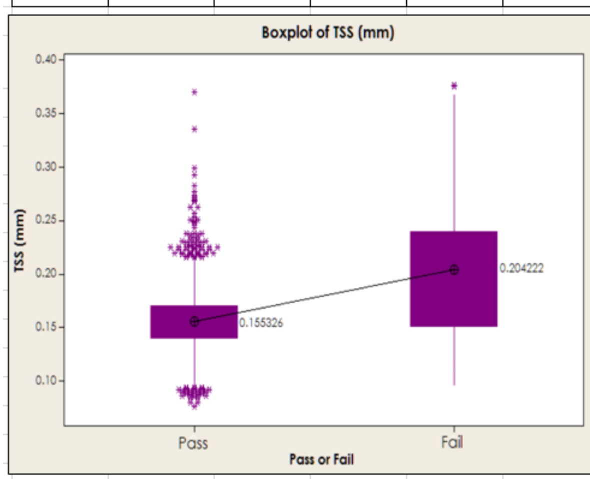

Figure 20. Plot of Coplanarity vs Test Result

The Second part of the analysis was to match the ICT test results with each of the variations to see which actually had an effect on the outcome. Contingency tables were created for comparing variations based on build quantities and failures. A Pearson Chi Square analysis was run on each. The results showed that the suppliers, board materials and rail copper variations had no statistically significant association with failure rate. Despite showing better performance in one of the groups for flatness the copper balance was in the PCB showed no difference between existing and modified boards.

The 2 attributes found to have statistically significant association with failure rate were the position in the working panel where boards from the non-corner panels showed a higher yield and the change to the board breaks where modules with the additional breaks moved to the corners had no defects as shown in Tables 9 and 10.

Table 9. Analysis of Panel Position

Working Panel Position Contingency Table

		0 Pass	1 Fail	Total
Corner boards	Row count	512	16	528
	Row percent	96.97	3.03	100
Non corner boards	Row count	2680	20	2700
	Row percent	99.26	0.74	100
Total	Row count	3192	36	3228
	Row percent	98.88	1.12	100

Pearson Chi-Square = 20.993, DF = 1, P-Value = 0.000

Likelihood Ratio Chi-Square = 15.855, DF = 1, P-Value = 0.000

Table 10. Analysis of Board Tabs

Break Tab Contingency Table

		0 Pass	1 Fail	Total
Current tabs	Row count	2586	36	2622
	Row percent	98.63	1.37	100
Extra tabs	Row count	606	0	606
	Row percent	100	0	100
Total	Row count	3192	36	3228
	Row percent	98.88	1.12	100

Pearson Chi-Square = 8.414, DF = 1, P-Value = 0.004

Likelihood Ratio Chi-Square = 15.064, DF = 1, P-Value = 0.000

CONCLUSIONS

Phase 1

The evaluation determined that the incoming PCB coplanarity had an impact on the yields of the assembly of the module to the carrier. Panels sorted into group a demonstrated a lower PPM than those in the B and C groups The PPM defect levels rose significantly in Group B and nearly doubled in Group C. Group A had a lower average coplanarity than those in Groups B and C. Despite the sorting the sorting at the panel level group a still had individual modules with high coplanarity values but at a lower percentage than the other groups.

Analyzing passing and failing modules PCB Coplanarity was found to have a statistical association to process yield. Passing modules were found to have a lower average coplanarity than failing modules.

In order to improve yields and eliminate board sorting improvements need to be made in the fabrication process by changing the design or material or a combination both.

Phase 2

Despite the consensus from PCB suppliers and the product development team the PCB material and copper balance had no statistically noticeable effect on the assembly yields. The balanced copper attribute may have been underrepresented due to the loss of the Supplier 1 samples and may warrant further investigation.

The board position in working panel was found to affect failure rate. Boards from non-corner locations displayed a better average coplanarity than those from the corners. This attribute may be difficult to change but will be investigated with PCB supplier.

Boards with more tabs located in the PCB corners were seen to have the largest impact to the carrier attachment success. Being a simple change to the panel this change can be easily implemented and monitored in larger lot sizes.

REFERENCES

[1] IPC-A-610 D Section

[2] JEITA ED-7306**,** Measurement methods of package warpage at elevated temperature, Section 3.6