Thinking Globally, Measuring Locally

Can a two-tier flatness specification provide relief?

Patrick Hassell

Within the PCB fabrication industry, specifications for finished board flatness continue to tighten. The primary driver behind this trend is the use of surface-mount devices. The strict co-planarity demands for these devices mandate a virtually planar interconnect region on the PCB. In order to assure the required flatness in a given local area, specifications are being applied across the *entire* PCB. The concept of a two-tier specification—one for global area (overall bow and twist) flatness and one for local area flatness—merits examination. However, several key issues will need to be explored and addressed. These include measuring and inspecting local and global flatness, maintaining this specification during thermal processing, and accounting for the flatness/behavior of the device itself.

The IPC standard for allowable bow and twist of bare boards has long been published at 1% (inch per inch). Despite this "rule of thumb," as it is probably more accurately referred, fabricators are seeing product orders with flatness requirements of 0.75%, 0.50% and some even at 0.30%. Traditionally, circuit board layout designs along with interconnect technologies have been much more forgiving on board warpage. Construction aspects of through-hole pins and the larger lead pitches of early stage surface mount devices made them more robust to mechanical variations on the board level. Assembly processes benefited from ample solder paste deposits and/or solder waves—each of which could compensate quite well for substrate warpage. Although warped boards were often the cause for component-substrate interconnect defects, warped boards tended to be more of a problem for handling and placement issues. Such global warpage symptoms included line jams, shingling, and card insertion problems.

Introduce fine-pitch technologies, multiple reflow processing, chip-carrier packaging, and so on, and take away a substantial amount of solder paste volume, and suddenly you have a whole new level of flatness concerns. Sub-0.020" pitch perimeter leaded packages, 500+ I/O area array packages, 3"+ long SMD connectors—each of these devices is critically dependent upon co-planar solder pads for assured interconnect. To illustrate, consider a 27 mm PBGA component. When being attached to its PCB, one can expect to deposit 0.006" to 0.007" (height) of solder paste. If the flatness specification on the PCB is 1%, it is possible that a 0.015" displacement could exist on the interconnect area and the board would still be within spec. [Diagonal of 1.08" square footprint = 1.53", 1% of 1.53" = 0.015]. Theoretically, the potential for solder joint defects is significant. Only by tightening the flatness specification can a designer or assembler enhance confidence that co-planarity will not be a problem. A 0.5% spec on the same example given above calculates a maximum allowable variance of 0.0075". Understandably, the process engineer is much more

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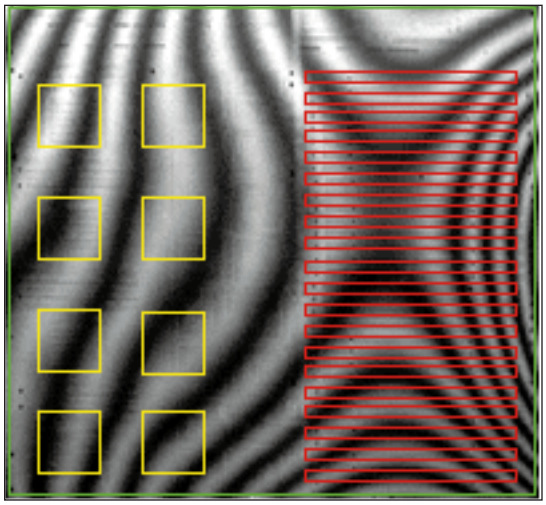

Figure 1. Shadow moiré test pattern of a 16" x 15" PCB. Figure 1a corresponds to the global flatness represented by the green outline. Figure 1b corresponds to the local area flatness of a BGA footprint represented by a yellow square. Figure 1c represents the local area flatness of a surface mount connector represented by a red rectangle.

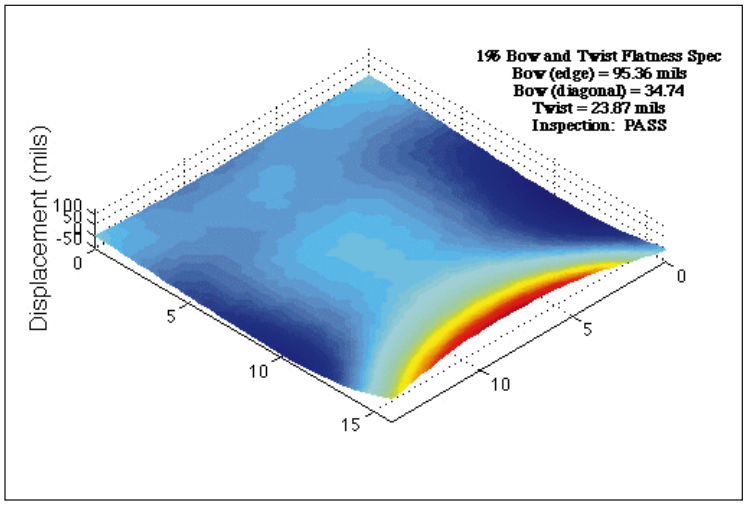

Figure 1a. Global PCB flatness represented by the green outline in Figure 1.

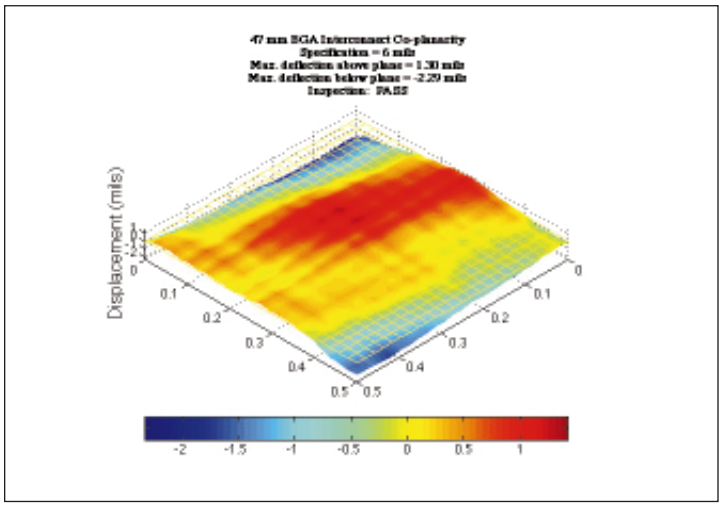

Figure 1b. Local area flatness represented by a yellow square in Figure 1.

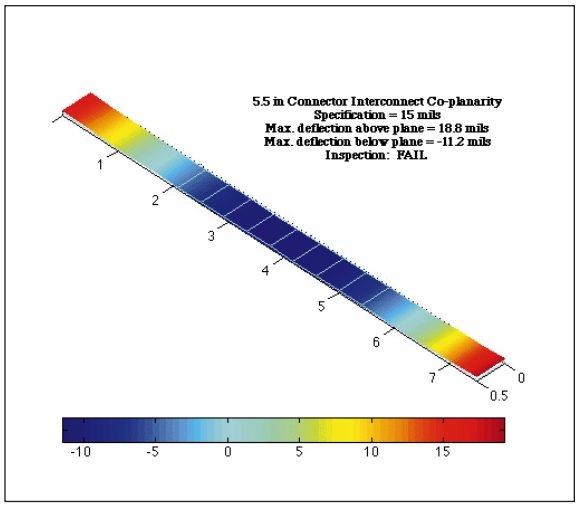

Figure 1c. Local area flatness represented by a red rectangle in Figure 1.

comfortable with these figures.

Non-spec boards can result in high defect and rework levels for assemblers and poor yields for fabricators. The impact of boards that do not meet flatness requirements is much greater today than it has ever been. Interconnect defects, material handling, and card insertion issues related to board warpage can translate into significant dollar loss. Non-value added rework processes such as flatness baking or materials and/or construction redesigns by the fabricator could easily destroy profit margins. Down time on automated assembly lines, assembly rework processing, damaged components—each costs assemblers a bundle.

Technological developments in the area of out-of-plane displacement measurement and analysis have created potential for a two-tier flatness specification. A specification of this nature would allow for very tight local area flatness requirements while relaxing the requirements for overall global flatness. Under such a format, for example, a given board design could be specified at 0.3% flatness at designated BGA device interconnect areas and at a 1.0% bow and twist requirement for the board as a whole. This would ensure that assemblers get the flatness they need in critical component areas while relaxing the overall tolerance for warp of the board. In theory, this should increase yields and reduce rework for both assemblers and fabricators alike.

The fundamental flaw with the existing flatness specification approach is that localized co-planarity measurements are not the average of global warpage. There is no guarantee that localized co-planarity will be repre-

sented by the average of a global (bow and twist) specification. This being said, it seems wasteful to rework and/or scrap perfectly functional boards that might fail a 0.75% bow-and-twist specification, but be well below localized co-planarity limits required for defect-free interconnect. At the same time, it seems unnecessary to process and assemble boards that pass a bow-and-twist specification but have localized co-planarity measurements that are known to cause defects.

Measuring Flatness

So you are ready to measure the local area flatness of a rigid board with pin gauges? Good luck. As much of a paradigm shift as a two-tier flatness specification would be, so too must be the method for measuring flatness. Inspection is viewed typically as a non-value added process for which no one desires to bear the responsibility. Especially when the result of an inspection is either a "pass" or "fail" reading. Only when an inspection process reveals quantitatively "how good" or "how bad" does it begin to provide value for the manufacturer. Statistical information on how flat finished boards are, provides a means for monitoring processes upstream, as well as for monitoring defects downstream. The ability to correlate changes in processes and materials to resulting board flatness for the fabricator becomes valuable for optimizing production. The ability to correlate soldering and assembly defects to board flatness for the assembler will help reduce rework.

Shadow Moiré Technique

Most existing methods for measuring bow and twist can not provide the level of precision, required information, and throughput necessary to perform a comprehensive analysis. While several alternative methods are available for characterizing the surface of finished boards, it is shadow moiré technique that has perhaps the best opportunity to satisfy the needs of the industry. Shadow moiré is an optical, non-contact technique that makes full-field measurements. Shadow moiré hardware integrated with high sensitivity analysis software allows for the generation of an out-of-plane displacement matrix that fully characterizes the board surface. It is then possible, through software applications, to analyze both the entire matrix and/or any subset areas of the matrix.

Other key benefits of shadow moiré are its speed—data acquisition at video frame rates—and its sensitivity —sub 0.0001" capability.

Shadow moiré has the potential to provide a means for the emergence of a two-tier flatness specification. By collecting surface topography data across the entire sample one can now set parameters for acceptance on both a local (i.e. area array device sites) and a global (i.e. bow and twist) basis. Information on the frequency, magnitude and location of warp for each sample becomes a valuable tool for SPC purposes at the fabricator. Additionally, the assembly process engineer is positioned to benefit by correlating specific defects to specific amounts and location of warpage. Once this is known, finished boards can be more effectively screened and, most importantly, processes can be more effectively monitored.

Thermal Loading

Assembly processing brings up another critical point in PCB flatness—thermal loading. In a perfect world, boards would arrive flat and stay flat. The composite nature of these substrates dictates a mechanical property set that is complex. Each of the respective materials used in the construction of the PCB is characterized by different mechanical property values—each of which changes according to temperature.

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Reflow processing is perhaps the most time-temperature intensive process a board will undergo. Flat boards that go in the front end of the reflow oven don't always come out flat on the back end. One qualitative opinion shared by many in the industry is that bare board PCBs do not tend to get better, with respect to flatness, as they go through reflow. If it is bad to start with, it will be worse when finished.

Thermally loaded boards exhibit design and temperature specific behaviors. Each reflow process in itself consists of multiple variables that can impact mechanical behavior of an assembly. Ramp rates, soak times, peak temperatures, cool-down rates, temperature gradients, and so on are common variables that can be set by the process engineer. Process parameters such as these can be optimized for best thermomechanical behavior for a given design by acquiring experimental data on the part during processing. Again, shadow moiré technique has capabilities in this field. Shadow moiré technique can be used in the laboratory

to perform in-process measurements of substrate warpage behavior.

Research indicates that bare boards exhibit very design- and/or process-specific behavior during thermal processing. In several specific cases, one trend that has good quantitative support is the following: while PCBs and substrates may vary (sometimes substantially) in global flatness from part to part, in most cases, the relative warpage behavior is often times consistent. For example, two parts are inspected and measured to have twist values of 0.010" and 0.025" at room temperature, respectively. The two parts are then measured for warp using shadow moiré technique during simulated reflow processing. The maximum relative (difference in measurement from initial state) twist value measured is often very similar. If a 0.015" relative twist occurred during processing, that would translate to an absolute maximum twist value of 0.025" and 0.040" for each of the respective parts.

A certain degree of mechanical integrity must be maintained between the area array device and the PCB substrate in order to ensure defect free interconnect.

If one knows the design- and/or process-specific thermomechanical behavior for a PCB, this information can be used to help set parameters for room temperature flatness specifications. Flatness parameters based upon high-temperature evaluation combined with local area and global area inspection capabilities could be used to effectively screen substrates to enhance defect free processing objectives.

Co-Planarity of Component Substrates

One key element to a two-tier flatness specification yet to be discussed is the co-planarity of component substrates. Of particular focus is the area array devices that were earlier identified as a key driver in the overall tightening of flatness specifications. Solder ball co-planarity specifications have been relaxed from 0.004" to 0.006" to 0.008". One must examine the value of a solder ball co-planarity measurement, particularly when it is quite often the substrate to which the balls are attached that dictates their co-planarity [Note: most published solder-ball height variances are in the +/- 0.001" range].

While it is the tops of the solder balls that define the interconnect plane for the BGA device, it is the substrate characterization that ultimately affects the solder balls' position. A laminate-based BGA substrate is essentially another PCB that exhibits a design and process-specific thermomechanical behavior.

As discussed with the PCB substrates, so too do similar measurement capabilities and mechanical behaviors exist at the package level. Quantitative in-process data points toward similar relative out-of-plane displacement behavior during processing. Additionally, data has shown that BGA laminate substrate warpage at temperature can sometimes be far worse than the PCB interconnect region. The fact of the matter is that there are now two independent systems—the PCB and the area array device—that each have a unique room temperature topography and a unique displacement behavior at temperature. These two systems must maintain a certain degree of mechanical integrity in order to ensure defect free interconnect.

Conclusion

Area arrays, large SMD connectors, multiple reflow processing, and mismatched CTEs are a few of the key elements driving the demand for flatter, more thermomechanically stable substrates. A better understanding of global and local PCB flatness and its impact on processing related defects stands to benefit fabricators, assemblers, and packagers alike. Isolation among design and engineering groups at these three levels needs to be greatly reduced in order to achieve this best. A technological means for acquiring the necessary data for quantitative analysis purposes exists today with shadow moiré technique. As industry trends continue toward higher I/O devices, more complex materials, and innovative processing, shadow moiré has the opportunity to provide the means for monitoring substrate flatness on both a local area and global area basis. Effective monitoring of local and global flatness could provide needed relief for fabricators and increased confidence for assemblers. **FAB**

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Patrick Hassell is business development manager with Electronic Packaging Services Ltd. Co., Atlanta, GA. He can be reached at eps@warpfinder.com.