Ready to Start Measuring PCB Warpage during Reflow? Why and How to Use the New IPC-9641 Standard

Ken Chiavone
Akrometrix, LLC
Atlanta, Georgia

Foreword by John Davignon
Chair, Printed Board Coplanarity Subcommittee (IPC-9641)
Davignon Consultancy, LLC
La Center, Washington

Foreword

In late 2011 there was a growing concern that the PCB industry was not keeping in step with the component substrates' need for flatter boards at elevated assembly reflow temperatures. This situation was showing up as lower assembly yields and higher rework for some components. The need to understand how the board reacts during assembly reflow was not being met by the existing IPC-TM-650 2.4.22 Bow and Twist test method. JEDEC had publications for components in place that set flatness requirements at elevated temperature but there were no corresponding publications for the board. This growing concern led a group of OEMs', EMS's, PCB fabricators and measurement equipment suppliers to form the IPC 6-11 Printed Board Coplanarity Subcommittee in early 2012. The time was right for a new look at board flatness and the committee developed and passed the IPC-9641 High Temperature Printed Board Flatness Guideline within a year from its' inception. IPC-9641 is a guideline and as such, was developed to provide a standardize methodology for evaluating board flatness at elevated temperatures so that the electronic industry can have meaningful discussion on the interaction between component and board at this critical time in the assembly process. It is the committee's hope that the PCB industry will start to collect the elevated temperature data on its products prior to setting any limits or specifications. This data will help OEM and PCB designers gain some fundamental knowledge of board movement and be prepared for any future board flatness requirements.

Introduction

The new standard "*IPC-9641 High Temperature Printed Board Flatness Guideline*" has been approved and released by IPC. In it, local area PCB warpage across reflow profile temperatures is addressed, for the first time by an international standards organization. The standard provides guidelines for selecting measurement equipment, planning testing, preparing PCBs for test, performing measurements across reflow temperatures, and reporting local area warpage results.

Why is this happening?

Measuring and controlling package warpage across the full thermal reflow profile has been standard practice for many years and is seen as critically important to final product yield. IPC-9641 has been approved because IPC members have determined that, as stated in the introduction to the standard, "…controlling the board flatness is equally important for preventing subsequent assembly-related issues including open or bridging joints which ultimately cause

product failure." Assembly-related issues also include challenging problems such as head-in-pillow that ultimately lead to field failures and product returns. So, while for many years the package was held up for scrutiny as the only relevant contributor to warpage-related assembly defects, now the other side of the attach interface, the PCB land area, has also been identified as a potential contributor to defective assemblies. **It's now important to understand, quantify, and control the warpage of PCB areas where packages attach, across temperatures.**

What good will the new standard do?

The standard is both educational about the general topic of PCB warpage measurement, and specific in its guidelines for how such measurement should be done. For the first time, there is a public, international standard for local area PCB warpage measurement across the reflow profile, and the contents of this standard can be built upon by companies to create useful detailed methods and procedures to share with their supply chain partners. The standard provides both a starting point and a point of reference as companies begin to build, or to improve their already existing, PCB warpage measurement systems. As an additional benefit, when dynamic warpage information is obtained from PCB areas, this data can be shared with those responsible for package manufacturing and SMT assembly, to facilitate continuous improvement in both component shape compatibility and final product quality.

The rest of this article consists of a summary of the contents of IPC-9641, followed by some notes about how to implement it using practical best practices derived from years of measuring packages and PCBs.

Summary of Section 1 – Purpose

The first section introduces the intent of the standard, explains its scope and how it differs from existing standards, and includes a glossary of terms which are defined to provide a common understanding of meanings of the warpage-related technical terminology that appears later in the document. For those already involved with warpage measurement, the glossary may serve as a useful reminder list, but for those not yet measuring warpage of any type, it may serve as an invaluable reference, since it lists other documents and standards (such as JEDEC JESD22-B112) that have led up to this standard, and are therefore useful to understand in order to get the most from it.

A concise statement of the purpose of IPC-9641 comes from its introduction: "This document aims to provide guidance on methods and procedures for critically evaluating printed board flatness during a simulated temperature reflow cycle."

Summary of Section 2 – Applicable Documents

This section is simply a list of all related JEDEC, IPC, and Joint Industry Standards, for serious students of the subject who want to review all available publications from these bodies that provide context for IPC-9641.

JESD22-B112 *"High Temperature Package Warpage Measurement Methodology"* is the most closely related standard on the list. It details a method for consistently measuring package warpage, like IPC-9641 addresses measuring the corresponding land areas on PCBs.

Summary of Section 3 – Measurement Instrument Requirements

This section reviews different metrology technologies and the theory behind how they work. It is the most purely 'educational' section of the document, and explains **shadow moiré, projection moiré, fringe projection, confocal, and optical coordinate measurement technologies**. These are the metrology methods that are 'recommended' in the standard, for PCB local area warpage measurement. (Each technology is only briefly discussed, and the pros and cons or trade-offs for each technology are not fully addressed, so this section is best used as an introduction to the topic of potential measurement technologies, and supplemental research would be prudent.)

Summary of Section 4 – Parameters of Interest

This section lists contributors to PCB warpage, including design and manufacturing variables. It notes that it is easier to change the manufacturing parameters than the actual design of the board itself.

The effects of clamping and board support methods are explored. Diagrams and statics equations illustrate the mechanical effects of constraining the PCB during reflow assembly. The purpose of this section is to emphasize the importance of mechanical support and clamping constraints as variables to be considered and dealt with appropriately when making decisions about warpage measurement methodology.

Summary of Section 5 – Recommended Test Methodology

This section includes recommendations for how to control variables that exist when making thermal warpage measurements on PCBs. Its subsections include:

1. Preconditioning/Preparation of Samples – replicate as close to production preparation as possible
2. Number of samples – use a minimum of six PCBs per test
3. Thermocouple Placement – attach with epoxy or Kapton® tape
4. Specific Temperatures for Data Acquisition and Ramp Rates – measure at temperatures across the reflow cycle, with ramp rates as high as possible with an acceptable temperature gradient
5. Recommended Test Methodology – includes an example reflow profile with measurement points shown
6. Data Reporting – provides example of 3d graphs with signed coplanarity gauges as results

Summary of Section 6 – Metrology Accuracy for Printed Board Flatness

This section provides an example method of how to verify that your measurement equipment performs accurately across all relevant temperatures. The process involves measuring the surface of a material that does not noticeably change shape as temperature changes (due to having a low coefficient of thermal expansion), at multiple temperatures across the reflow profile. The gist of this section is that there are ways to 'prove' that results from a piece of equipment are valid at all measurement temperatures.

How to Implement IPC-9641 at Your Facility

Because of customer request, assembly problems, quality assurance needs, or some other driver, you may need to start implementing the standard and begin measuring land areas on PCBs for warpage, across the reflow profile.

The general information and 'Best Practice' suggestions that follow apply to all the measurement technologies recommended in the standard.

Choosing Equipment

If you've already been measuring warpage at elevated temperatures, you're halfway to implementing the new standard. It's likely you'll want to utilize the warpage measurement system you have at hand. For those that don't have equipment to access, choosing the measurement, analysis, and reporting system you will use will be an important decision. Some things to keep in mind when evaluating options:

Desired z-resolution – Z-resolution is how closely the equipment can 'trace' the actual surface to deliver accurate data. It's usually defined in microns. For example, a system with 5 micron z-resolution would be able to distinguish between two points on a surface that had heights that were different by 7 microns, but a 3 micron height difference would likely not be measured (the height difference would be reported as 'flat'). Package designers and manufacturers typically desire a z-resolution in the 1-3 micron range. For PCB areas, 5 microns or less is recommended.
(For fringe-based systems, z-resolution is a function of fringe density. For confocal and other optical point-based systems, z-resolution is a function of their speed setting, optics, and the light source used.)

Desired data density (XY) – Confocal methods will provide slow point-by-point measurements, making the XY density of necessity low. While other optical methods can measure hundreds of thousands of points in 1-5 seconds, confocal is a scanning technique that can only deliver a few points in that amount of time. So the trade-off for extremely precise z-resolution is very poor xy resolution.

Expected volume of measurement – How many measurements will be required per day and the throughput capability of the system(s) being considered should be estimated. Typically, fringe projection and shadow moiré provide the fastest speeds, while confocal and OCM systems take much longer, as noted in the standard.

Planned correlation with suppliers and customers – The decision of what technology and specific equipment to use can become complicated, or sometimes simplified, when the capabilities and plans of your supply chain partners are considered. If there is intent to share data amongst multiple parties, it would be appropriate to make a group decision about what measurement technique will be used and what data correlation format will be shared.

Accuracy at High Temperatures

Once you have acquired your measurement system and understand how to use it, IPC-9641 recommends that you verify its accuracy across temperatures. The standard includes a guideline for how to establish its accuracy capabilities, so you may want to: 1.) See results from your equipment vendor of their results of their standard 'accuracy across temperature validation' and 2.) Perform additional validation testing at your facility, on your equipment. The IPC standard is called a guideline for a reason, and intentionally does not attempt to detail system-specific methodologies. Your equipment supplier will likely have a more complete and detailed methodology that you can use that includes information such as proper sample surface preparation, safety protocols, etc. to use when establishing the accuracy of the equipment at elevated temperatures.

Preparing PCB Samples for Test

After you are comfortable with the measurement accuracy across temperatures that your measurement system delivers, you will be ready to prepare samples for test.

The IPC-9641 standard notes that, depending on their moisture levels, PCBs may require a pre-bake process. From our experience over the last decade, and from testing many PCB designs during a PCB flatness study for iNEMI from 2009 to2011, we know that board moisture is a major contributor to warpage results, and you should seriously consider establishing a 12 hour pre-bake to remove moisture from the boards to a consistent minimum level. This process will help you control one of the variables that has a large effect on thermally-induced warpage. Alternately, if there is no pre-bake that occurs before actual production reflow assembly, establishing the wider range of warpage and higher coplanarity results that represent assembly conditions may be a better approach. Across the package industry, pre-baking is the norm, especially since pre-baking and/or controlling package moisture levels with in-transit sealed shipping bags prior to assembly is common practice. Just keep in mind that warpage levels will be much more in-control and consistent if the boards are pre-baked before measurement.

Best Practice: A 12 hour pre-bake at 125°C is recommended for all PCBs.

Painting the Surface

Most of the measurement technologies listed in IPC-9641 do not absolutely require sample surface preparation, i.e. painting them white. However, it is a fact that when using optical metrology, the best data

possible (the data that best represents the actual physical surface being measured) results from the most ideal optical surface. And the most ideal surface, for optical measurement, is diffuse and white. Unpainted surfaces yield results with more noise, and in some cases 'garbage results' if the surface has too much specularity, such as with shiny copper traces or pads. Correlation will be much improved if all parties involved follow the same sample surface preparation method. Your equipment supplier can recommend sample surface treatment steps to help you get the best data.

Best Practice: Painting the 'area of interest' flat white is recommended.

Cutting the Boards

To measure the package land area on the PCB, the PCB must fit into the oven of your measurement equipment. If you have a board that is larger, trimming the board to fit is required. The rule of thumb is that the more material around the area of interest that you can keep, the more 'real' warpage results you will get. Cutting the boards should be done with an attempt to induce as little mechanical and thermal stress as possible, such as by clipping them with shears.

Best Practice: Carefully trim the board to fit in the oven.

Attaching the Thermocouples

The standard notes that high temp epoxy or Kapton® tape are the preferred thermocouple attachment methods. A picture of the taping method, just off the side of the painted land 'area of interest', is shown in Figure 1.

Best Practice: Attach the driving thermocouple near, but outside, the package land area to be measured.

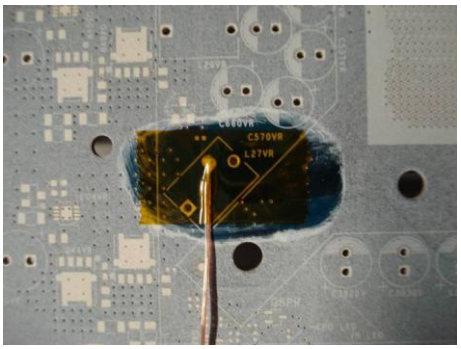

Figure 1 - Thermocouple attached with Kapton® tape

Fixturing the Samples

The standard notes that there are various assembly fixturing techniques used in reflow assembly, including simple on-rails, simple supported (with at least one rail across middle), and different clamping methods.

Not fully covered in the standard is what to do about measuring the boards if they are normally clamped during assembly. This is especially relevant, since clamping the boards does affect warpage, and putting a board that is in a clamping fixture into the oven of your measurement equipment will likely not work, if the fixture blocks heat transfer to the board. Many, but not all, measurement systems use IR heating, and if the clamping fixture blocks radiated energy, it will not be possible to measure the PCB 'in situ' with the same mechanical constraints in place as when it goes through the reflow oven. Measuring with a simple support setup and using that data to correlate with what the area will

actually do when clamped is one alternate approach. However the sample is supported in the oven, with two or three rails, on a flat glass sample support, a specialized fixture as shown in Figure 2, or in its own clamping fixture, this set-up should be established and communicated with all the supply chain partners in your correlation group.

Best Practice: Fixture boards consistently for all measurements.

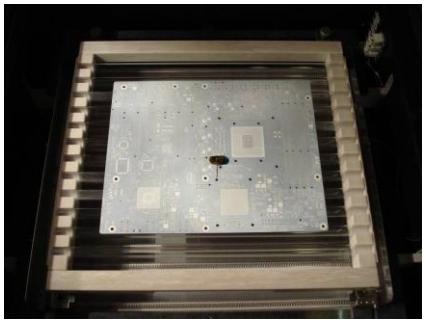

Figure 2 - PCB in oven on Uniform Area Support (UAS) Fixture

Establishing the Thermal Profile and Measurement Temperatures

Another method you should share with all your supply chain partners interested in board warpage is the thermal profile and measurement acquisition points you will use for each board design. Comparing results both between and within board designs, for different regions of interest, is facilitated by establishing a common set of temperatures that are important for decision-making. Measuring at multiple points is prudent, but it can become impractical to attempt to measure at every single degree, for example, since temperatures are changing quickly and each measurement takes some non-zero amount of time to complete.

'Ramp rate', or rate of change of temperature of the sample, is mentioned in the standard. The standard recommends a ramp rate set as high as possible, that does not induce more than a 10 degree Celsius difference between the top and bottom of the sample. In our experience, a 0.5-1.0 degree/second heating rate is ideal, though with thicker boards, which tend to impede temperature equalization, the target rate will need to be established with actual test results per board design.

Best Practice: A typical temperature profile with acquisition points is shown in Figure 3. Adjust heating rates to minimize temperature differentials.

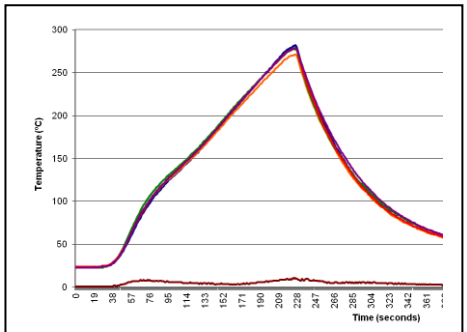

Figure 3 - Thermal Profile Charting Measured Temperature of Sample vs. Time

Taking the Measurements

After all this preparation, it's finally time to take some measurements. The board is in the oven, the profile is set, you run the automated acquisition software, and the machine does the rest. An example of raw data from a PCB land area, measured with shadow moiré technology, is shown in Figure 4.

Best Practice: Run the thermal profile, and obtain measurement data only at important temperature points.

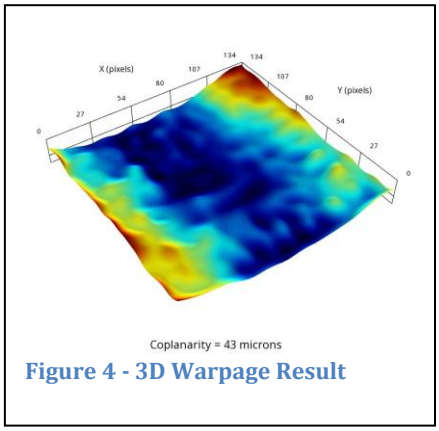

Figure 4 - 3D Warpage Result

Analyzing and Reporting the Data

Analyzing the raw data results by following a common method is required, if data is to be correlated with other parties. The amount of data smoothing, data density, and other variables need to be controlled as closely as possible, to get the closest resultant correlation. Preparing results in a table or 3D visual reporting format are common ways that package suppliers communicate dynamic warpage. With enough samples measured throughout a temperature range, and associated analyses run, this complete process is sometimes called the 'warpage characterization' of components such as packages and PCBs.

Best Practice: Process data according to a common methodology shared amongst your supply chain partners. Create template-based reports to share.

Number of Samples

Establishing a statistically acceptable set of results will depend in part on how many samples are tested, of a given lot of a particular design. The standard recommends testing a minimum of six PCBs to establish the performance characteristics of the lot, though testing more may give a higher confidence level that a representative range and standard deviation have been properly established. The warpage 'tendency' of a particular PCB lot is usually clear once ten samples have been measured.

Best Practice: Test 6-10 boards per lot, to effectively 'characterize' the lot's expected warpage across temperatures.

Conclusion

In April of 2013, the Global SMT&Packaging article titled "Two Surfaces are Better than One" illustrated a method for analyzing the interface between attach surfaces, using two 3D surfaces measured at temperatures across the reflow profile. By releasing *"IPC-9641 High Temperature Printed Board Flatness Guideline"*, IPC has indicated to all of us involved in the SMT industry that making assumptions about the warpage of one side of that interface, the package land area on the PCB, is no longer sufficient for the design of current and future reflow assemblies. As suggested in the prior article, we are moving toward a time when the shapes of the components attaching during reflow will be compared and constrained at each temperature, and the compatibility of those shapes will tell us what needs to be done to get the best product yield, as well as what final quality level we can expect from their combination. Measuring the

reflow-induced warpage of package land areas on PCBs is a big step in that direction.

[IPC publishes released standards on its website, at www.IPC.org.]

***

Acknowledgements:
Information about thermal warpage measurement best practices in this article was provided and reviewed by the subject matter experts at Akrometrix, Ryan Curry and Neil Hubble.

Author Notes:
Ken Chiavone is Vice President of Engineering for Akrometrix, LLC. For more than ten years he has led the development of equipment and software products for the medical and electronics industries, and is currently writing a book about Warpage Management.