New Package/Board Materials Technology for Next-Generation Convergent Microsystems

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Abstract

Current printed wiring boards (PWBs) are all organic, the most common being epoxy-glass laminate FR-4 due to its cost effectiveness and overall performance. However, for high-density wiring (HDW) and assembly of flip-chips directly to the substrate without the use of underfill, substrate materials with low CTE and high elastic modulus are needed. Novel low CTE-high stiffness organic (carbon-epoxy) and inorganic boards (carbon-SiC) have been evaluated for flip-chip on board technology without the use of underfill. Standard liquid-liquid thermal shock tests were carried out on test vehicles with different board materials. In-situ warpage measurements and optical microscopy were used to analyze the observed failure modes.

The low CTE low stiffness ceramic and organic boards did not fail from solder joint failure but from cracking in the dielectrics and copper wiring. The high stiffness (>350 GPa) ceramic boards did not fail even after 1000 cycles. The failure modes indicate that a combination of high dielectric stresses and warpage results in crack propagation in conventional epoxies. The novel high stiffness low-CTE ceramic (C-SiC) is also processable in large-area at low cost and is hence a promising board material for future microsystems.

1. Introduction

The system-on-a-package (SOP) design paradigm provides a package level integration of digital, RF/analog, and opto-electronic functions. Two major components of SOP are sequential build-up of multiple layers of conducting copper patterns with interlayer dielectrics on a board and multiple ICs flip-chipped on the top layer. A wide range of passives, wave-guides, and other RF and opto-electronic components are buried within the dielectric layers [1]. The interleaved Cu and dielectric layers also support the high density interconnects for power and signal requirements. The board material should therefore meet certain electrical, thermo-mechanical reliability, HDI processing, and cost requirements.

Reliability of a SOP assembly is affected by the thermomechanical stresses induced in the package due to the CTE mismatch between the die and substrate and the build-up materials. A silicon die has an approximate CTE of 2-3ppm/^{o}C, while the conventional FR-4 substrate has a CTE of approximately 18-20 ppm/^{o}C [1]. Though underfill materials are being used to enhance flip-chip reliability, they impose several bottlenecks to accomplish high component density, fine pitch and unlimited I/O connections. Therefore, there is a pronounced need to evaluate board materials with CTE close to that of Si for reliable flip-chip on board without underfill.

The thermomechanical stresses due to CTE mismatch in the system result in solder joint failure, die cracking and delamination of the solder bumps and cracking of the build-up layers, leading to the failure of the assemblies. Stress management, therefore, has been an essential aspect of microsystems.

This paper assesses the reliability of candidate base substrate materials in comparison to conventional FR-4 boards. A novel large-area processable ceramic composite (C-SiC) board has been developed and evaluated for its flip chip reliability without underfill. The failure modes were studied by optical microscopy and in-situ warpage measurements.

2. Experimental

***C-SiC Board Manufacture*:** Composite panels of carbon fibers and a silicon carbide matrix are formed from commercially available carbon fiber fabrics and felts and a liquid polymeric ceramic precursor. The polymeric precursor is a highly branched polycarbosilane, which decomposes on firing to 850°C to give amorphous silicon carbide. Hydrogen is the main byproduct of the pyrolysis and is diluted and vented to the outside. In a typical preparation, layers of felt or fabric are cut to the desired size and shape, soaked in either the polymer or a slurry of polymer and silicon carbide powder. Hot pressing using light pressure (60 - 300 psi) gives flat panels up to 10" x 10" square with porosities ranging from 20 to 50%. To improve strength and stiffness, the panels are re-infiltrated with the polycarbosilane and the pyrolysis repeated until the porosity is below 5% (8 to 10 cycles). Planarity is best maintained if the panels are held flat under light pressure (1 to 5 Psi) during these re-infiltration/pyrolysis cycles.

To give the pore-free and planar surface required for wiring boards, the panels are lapped briefly and a paste

polycarbosilane/silicon carbide powder worked into the surface. The panel is then pyrolyzed and given two polymer infiltration/pyrolysis cycles to insure a pore-free surface. The surface of the panels is finished with a light lapping. The properties of fabricated panels are summarized in Table 1.

Fabrication of Test Vehicles: Test vehicles were fabricated using the sequential build-up process. Continuous unidirectional (Toray) and discontinuous carbon fiber (CCS) reinforced epoxy composites, FR-4, high stiffness ceramic (Cer2) and low stiffness ceramic composite (Cer1) were used as the candidate base substrates for the test vehicle. FR-4 test vehicle was used as a standard for comparison. Carbon fibers have ultra low CTEs and high moduli, so their reinforcement in polymers seems to be a promising solution to get low CTE and moderate stiffness boards. These boards are inexpensive, have easy machinability and large area processability. To evaluate the increase in reliability performance of boards with CTE close to that of silicon, test vehicles were fabricated both with and without underfill. The properties of candidate boards are summarized in Table 2.

Figure 1 shows the structure of test vehicle and process steps during the fabrication. The fabrication was done on boards with dimensions varying from 10-12 cm, each side. The carbon-epoxy substrates were initially roughened by Reactive Ion Etching for better polymer adhesion. Two different thickness (10 and 25 microns) of epoxy (CIBA 7081, Ciba-Geigy) layer were spin-coated on the substrate to provide the first insulation layer. Electroless copper plating was done using Shipley's process and the copper wiring was subsequently electroplated up to 12 microns. The ceramic composite test vehicles were fabricated with RCC (resin coated copper) lamination using Matsushita's (Koriyama, Japan) R0880 multilayered PCB materials. The RCC foil has 60-70 microns thick dielectric.

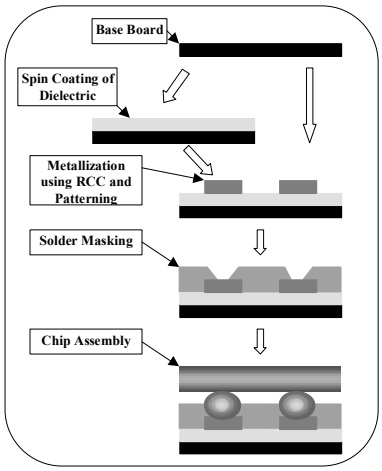

Figure 1: Flow chart for test vehicle fabrication.

The final solder mask coating (25 microns) was done with Taiyo solder mask (PSR 9000 A02 series) composition. Bumped PB-8 dies (Flip-Chip Technology, Practical Components, CA) were assembled on the board with conventional flip-chip process both with and without underfill materials. A commercially available fast-flow, snap-cure underfill (Dexter 4531, Loctite Corporation) was used.

Reliability Test: The reliability was evaluated with liquid-liquid thermal shock tests. Test vehicles were subjected to a thermal shock between -55^{o}C to 125^{o}C using liquid media. The thermomechanical reliability of the electrical interconnections was evaluated.

Shadow Moiré in-situ Warpage Measurements: The in-situ warpage measurements on the test vehicles during the thermal cycling were done at Akrometrix LLC., Atlanta, using the TherMoiré@ measurement system. This is an optical, temperature-dependent measurement system based on the Shadow Moiré technique, and includes automated phase stepping analysis. This non-contact full field measurement method generates a Moiré pattern of light and dark regions produced by the superposition of two regular motifs that geometrically interfere. A grating shadow, which distorts in the presence of surface warpage, is produced on the specimen when a collimated light source is directed through the reference grating. The specimens were supported with two parallel metal rods at each end to ensure free expansion in all directions. A grating density of 100 lines/inch with a resolution of 10 mils/fringe and a phase stepping sensitivity of 0.1 mils was used. The prescribed thermal cycle imitated the standard liquid-liquid thermal shock test (-55 ^{o}C to 125 ^{o}C but at a slower rate of 1^{o}C/min. Test vehicle fabrication for the shadow-moiré and reliability measurements was exactly the same. Liquid nitrogen was used to cool the samples to –55^{o}C. All boards are of dimensions 12 cm x 12 cm except for Toray board which is 10 cm x 7.5 cm.

3. Results and Discussion

C-SiC Fabrication: The main aim of this part of project is to achieve very high modulus. There is a trade-off between high modulus and high flexural strength; as the composites are made stiffer they also become more brittle. Current work to increase stiffness without causing embrittlement includes optimizing the panel's fiber architecture and using both higher modulus fibers and higher slurry loadings. Future work in this direction is to explore methods for obtaining the required low porosity with fewer re-infiltration cycles (currently 8 to 12 are required) and retaining greater planarity throughout the process so that less lapping is required to finish the plate.

Reliability Test: Thermal shock tests for flip-chip on board both with and without underfill were done on 5 different boards with different CTEs and elastic moduli. In order to understand the failure mechanisms, failure mode analysis was done using optical microscopy.

Several types of failure modes namely solder joint cracking, solder joint delamination, dielectric cracking, underfill and die cracking have been observed in the test vehicles. Conventional base substrate material FR-4 has been observed to fail within the first 100 cycles without underfill. As expected, the failure occurred at the solder joints due to the huge CTE mismatch between the Si die and the board. Test vehicles with underfill have been observed to sustain up to 1800 cycles as the underfill redistributes the stresses in the solder joints. Test vehicles built on low CTE

substrates with low modulus (~100 GPa) also fail at early stages of thermal cycle, both with and without underfill, the mode of failure in this case predominantly being dielectric cracking. For organic boards, solder joint cracking was also observed. The low CTE of board results in a high CTE mismatch between the dielectric and board which generates high stresses in the dielectric causing it to crack. In addition, the low stiffness causes the boards to warp during thermal cycling leading to solder joint delamination. The cracks in the dielectric propagate into the copper lines breaking the electrical continuity and thereby leading to failure of the assembly as shown in Figure 2. It can be noticed that for the carbon cloth reinforced epoxy substrate (CCS), reliability is quite low though effective CTE mismatch between the die and the board has been eliminated.

The unidirectional carbon - epoxy boards (Toray) with a higher modulus (~180 GPa) show similar failure modes though they fail at a later stage than board A, both with and without underfill.

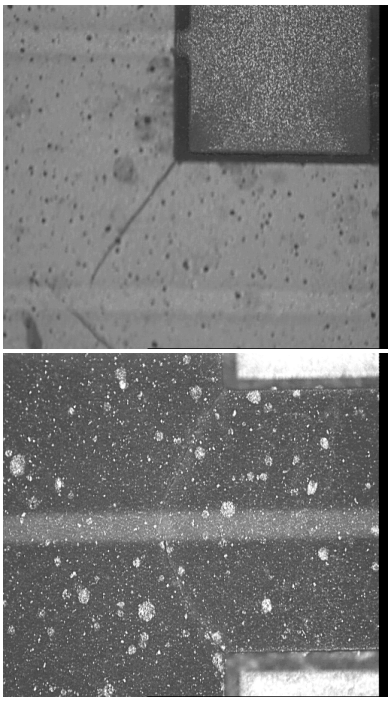

Figure 2: Failure modes in carbon-epoxy boards.

The ceramic composite board (cer1) did not show any failure in the solder joints even after 500 cycles because of its close CTE with that of Si. The flip chip daisy chain is completely connected though some of the pads showed high resistance implying that the failure was within the lines and not in the solder joint connected through the daisy chain. The warpage in these boards is lower compared to the organic boards because of its stable mechanical properties and absence of glass-transition temperature seen in epoxy boards. However, severe dielectric cracking is observed at the corners of the solder mask openings near the testing pads and along the edges of the solder mask openings. These cracks were also seen to penetrate through the copper lines. Cracks within the copper lines, independent of dielectric cracking were also observed within the solder mask openings as depicted in Figure 3.

The stiffer ceramic board which is a low CTE-high stiffness (350 GPa) board has good reliability both with and without underfill and does not crack even after 1800 cycles as evident from Figure 4. It was also seen that the boards with lower thickness of dielectric did not show any cracking after 1800 cycles while boards with thicker dielectric cracking showed small cracks at solder mask corners after 500 cycles. The thermomechanical reliability test results and failure modes are summarized in Table 3.

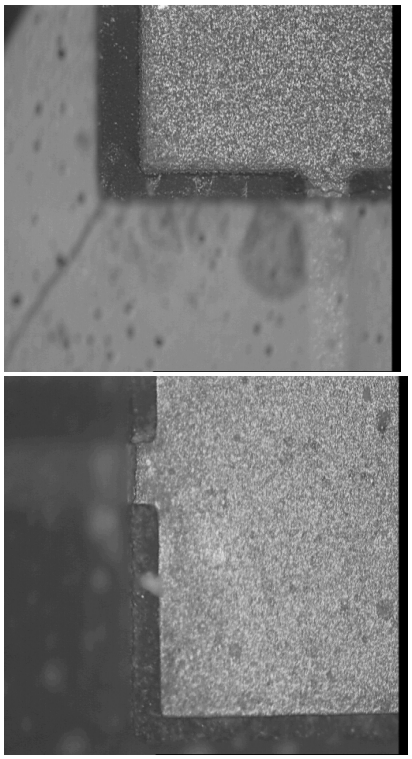

Figure 3: Failure modess in low stiffness ceramic boards.

Shadow Moiré Measurements: To further analyze these failure mechanisms, in-situ warpage was measured to monitor the board behavior during thermal cycling. CCS Carbon boards, which have a low stiffness, warp most during thermal cycling showing an out of plane displacement of as high as ~27 µm/inch board. On the other hand, high stiffness ceramic board (Cer2) shows negligible warpage of about ~3-4µm/ inch board. Conventional base substrate material, FR-4, also shows considerable warpage ranging from 7-12 µm/inch board over the cycled temperatures (-55 to 125) C. The experimental results are shown in Figure 5.

The ceramic composite board with 80 GPa stiffness showed a warpage going from a minimum of 6.5 µm/inch at 100 °C to 13 µm/inch at -55 °C. The Toray boards when cycled from 27 C to 125 C showed a warpage ranging from 6 to 1 µm/inch. These numbers are correspondingly lower compared to that of CCS boards. In the ceramic composite board Cer1, dielectric cracks were only seen at the corners and interfaces, which presumably are stress concentration regions. The large dielectric cracks which cut through the copper lines in CCS boards were not observed here.

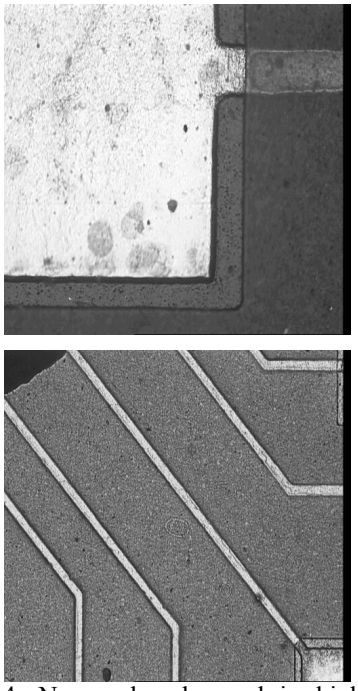

Figure 4: No cracks observed in high stiffness ceramic boards with 10 μm epoxy and solder mask build-up.

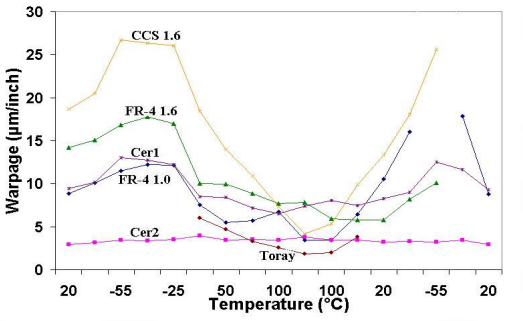

Figure 5: In-situ warpage measurements. Cer1: Low stiffness ceramic; Cer2: High stiffness ceramic.

Analytical models predict similar dielectric stresses for all the low CTE boards with CTE ranging from 1-5 ppm/C [2]. The dielectric cracking phenomena is insignificant in the high stiffness ceramic boards while the cracks in the low stiffness boards are more severe and lead to electrical failure. Hence, it can be inferred that a combination of warpage and dielectric stresses initiate these failures. Conventional brittle epoxies with low elongation to failure (low toughness) low strength, high CTE mismatch and high stiffness may not be the right candidate dielectrics for these boards. Dielectrics which lead to lower stress and have higher strength and toughness are required. Table 4 compiles the mechanical properties for some candidate SOP dielectric materials. While the electrical properties dictate that low loss dielectrics like BCB are needed for high-frequency and high-speed applications, the thermomechanical properties also need to be considered for proper selection of the dielectric materials.

4. Conclusions

This paper evaluates low CTE organic and inorganic board materials with a range of stiffness for reliability with and without underfill. While the solder joint stresses can be eliminated with boards having Si-matched CTE, the dielectric stresses and warpage result in the failure in these test vehicles. Hence, in-situ warpage of different boards was characterized with shadow-moiré technique and is correlated with the observed failure phenomena.

The results show that the failure in the flip chip test vehicles originate from cracks within the dielectric and copper lines, and the cracking corresponds to the measured warpages during thermal cycling.

The high stiffness ceramic boards did not fail after the thermal shock test. These ceramic boards can be manufactured in large-area using a low-cost processing technique and is hence an ideal candidate material for future SOP substrates.

Acknowledgements:

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References

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Table 1: Properties of the fabricated ceramic matrix composites.

Property	**Current board properties**		**Project Goal**
	Set 1	**Set 2**	
Thickness	2 mm	2 mm	1 to 0.5 mm
CTE	NA	3.0 ppm/°C	2 - 4 ppm/°C
Modulus	190 GPa	100 GPa	> 350 GPa
Flexure strength	50 MPa	300 MPa	Panel cannot be brittle
Planarity	+/- 50 microns	+/- 50 microns	+/- 5 microns
Panel Size (finished)	5" x 5"	5" x 5"	18" x 24"

Table 2: Constituents and properties of boards.

Candidate Substrate	Cloth	Filler or short fiber	Cloth Content (Vol %)	Matrix (Vol %)		Properties	
				Resin	Filler	CTE (ppm/°C)	Modulus (GPa)
FR-4	Glass Cloth	None	47	53	0	16	18.2
Carbon Short Fiber/ Epoxy Resin (CCS)	None	Carbon Short Fiber	None	48	52	2.9	100
Uni Dir. Fiber 0°/90°/Epoxy Resin (Toray)	Uni Dir. Fiber 0°/90°	None	60	40	0	0.5	180
High Stiffness Ceramic (Cer 2)	*	*	*	*	*	4	350
Low Stiffness Ceramic (Cer 1)	*	*	*	*	*	3	80

Table 3: Reliability Test Results.

Substrate	CTE (ppm/^{o}C)	Modulus (GPa)	Failure Mechanisms	Underfill	Cycles for failure
FR-4	16	18.2	Solder Joint Cracking	No Yes	100 1800
CCS	5	100	Dielectric cracking; Solder joint delamination	No Yes	100 200
Toray	0.5	180	Dielectric Cracking	No Yes	300 400
High stiffness ceramic (Cer 2)	4	350	-	No Yes	1800 1800
Low stiffness ceramic (Cer 1)	2-3	80	Dielectric Cracking; Copper line cracking and cracks along solder mask openings	No Yes	400 500

Table 4: Mechanical properties for some candidate SOP dielectric materials.

Material	CTE, ppm/C	Mod. GPa	Strength; Failure to elongation
Epoxy	60	3.5	30-83 MPa; 2-10 %;
BCB	45-50	2.5	87 MPa % ; 8 %
Avatrel	83	1	50-60 MPa; 20 %;
Siloxane	55	2.5	
Low CTE Polyimide	10	6-9	200-390 MPa; 15-34 % ;