Industry Trends Driving Need for Warpage/Flatness Specifications

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INTRODUCTION

Investigation of the thermomechanical behavior of devices and substrates began to gain in importance with the development of area array devices – most notably the BGA. Today, packagers and assemblers are faced with a multiplying amount of packaging formats and advanced substrates from which to choose. While debate may linger on which format is best, there is no question that the mechanical behavior for any given design is ever more critical. Temperature-dependent warpage evaluation of devices and substrates is proving to have significant value not just in the design and reliability phases, but also in the role of production diagnostics and production yield improvement.

INDUSTRY TRENDS

There are two key industry trends that are driving the need for warpage measurement (more specifically, temperature-dependent warpage measurement): the drive towards finer-pitch (1.0mm and less) devices and the move to lead-free solder.

Solder bond integrity is becoming more difficult in finer-pitch devices, primarily because solder paste volumes are smaller. As a result, there is less tolerance for package warpage, particularly in packages 40mm square and smaller. Today, there is the ability to ensure solder ball coplanarities of less than 50 micron (2 mil). This is, however, dwarfed by the overall package substrate coplanarity, which in some cases can be 500 micron (20 mil) or more. In addition, larger packages will have larger coplanarities, generally speaking. Therefore, as we move to finer pitches on larger areas, warpage (for both BGA substrates and bond pad sites on PCBs) is far outweighing solder ball coplanarity in importance.

In the PCB arena, the industry is now recognizing that traditional warpage measurements (bow and twist) – while important metrics for global characterization – are greatly complemented by local area flatness analyses. Local-area flatness measurement is coming to the forefront as an extremely relevant metric, with excellent correlation to solder bond defects. To illustrate this, Figures 1-3 demonstrate a PCB that has passed global flatness specs, but failed the more important local-area flatness spec for a surface mount connector:

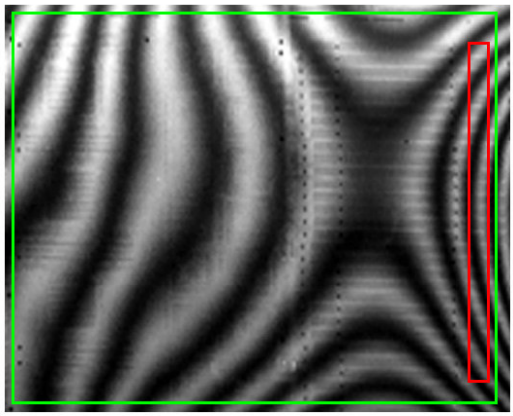

Figure 1: PCB with shadow moire fringe pattern. Green section denotes global area; red section denotes local-area region for surface mount connector.

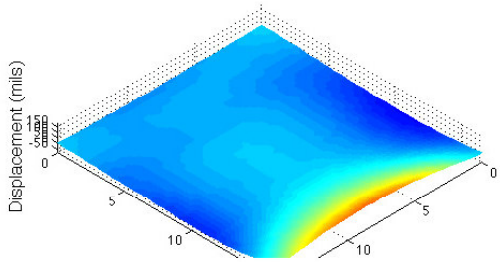

Figure 2: 3-D plot of global surface area; this board passes the global area coplanarity spec (80 mil measured coplanarity vs. 140 mil spec).

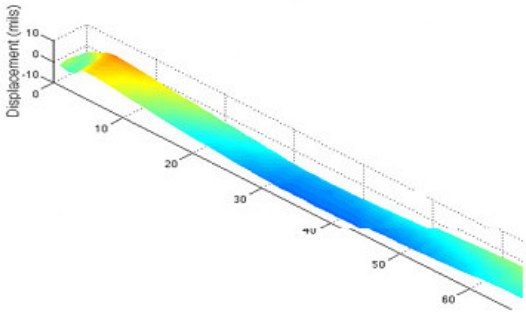

Figure 3: Local-area region fails spec for flatness (9 mil measured coplanarity vs. 5 mil spec).

Going one step further, temperature-dependent warpage measurement is superior to simple room temperature analysis, because warpage becomes exacerbated at elevated temperatures during reflow processing. Thus, the ability to replicate reflow profiles while taking real-time warpage measurements is ideal for package and substrate characterization. The emergence of lead-free processing (as well as bromine-free laminates and the drive towards thinner substrates) is further driving the need for warpage characterization and control. In most cases, as BGA substrates and PCBs are subjected to higher processing temperatures (~260C), the coplanarity values increase due to CTE mismatches between component materials. This increase in warpage has a direct impact on solder bond coplanarity. Figures 4 and 5 show how an increase in temperature from 220C to 246C can have a dramatic effect on coplanarity of the PBGA. In this specific case, there was a 56% increase in coplanarity over just a 26C change in temperature (data captured using a temperature-dependent shadow moiré warpage measurement system).

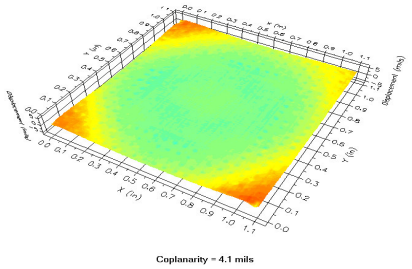

Figure 4: 27mm PBGA at 220C.
Coplanarity = 103 micron (4.1 mil)

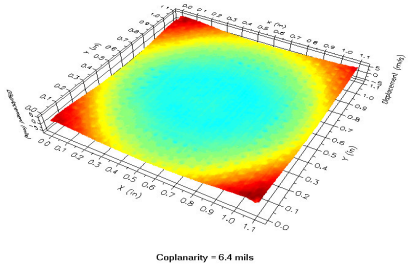

Figure 5: 27mm PBGA at 220C.
Coplanarity = 160 micron (6.4 mil)

THE SHADOW MOIRE TECHNIQUE

There are a variety of flatness measurement techniques available; however, very few offer temperature-dependent warpage measurement. As stated previously, real-time warpage characterization of packages, substrates and PCBs over a reflow profile is ideal, as this is the most crucial time for successful solder joint connectivity. One such technique that can measure warpage over a reflow profile is the shadow moiré method. Shadow moiré is particularly well suited for this because of its simple design/setup and flexibility.

The shadow moiré technique allows for the measurement of the topography of the surface of a solid object, *i.e.,* its deviation from a planar surface. It is a full-field, non-contact technique with data acquisition times of about one second. The technique has been in existence for decades; however, in the early 1990s, a technique was developed at the Advanced Electronic Packaging Laboratory of the Georgia Institute of Technology, which combined shadow moiré with a heating source. This allowed for real-time warpage measurement of substrates in a dynamic temperature environment. Actual samples could be driven through a designated temperature profile (IR/convective reflow, wave solder, curing cycle, harsh environment, etc.) and data is taken at video frame rates. The technology was developed under the direction of Dr. I. Charles Ume with industrial sponsorship. In 1994, at the request of industrial sponsors, the technology was licensed and formally commercialized.

Since then, shadow moiré has become the technique of choice for temperature-dependent measurement of packages and boards. The technology has been improved significantly, now offering sub-micron resolution and temperature capabilities from –55C to 300C. The technology now has worldwide penetration, and standards committees have implemented it as the de facto method for temperature-dependent warpage measurement.

INDUSTRY RESPONSE

As the finer-pitch devices and the lead-free initiatives take hold, industry has reacted to the warpage issue in several ways. Major corporations are beginning to see the value in temperature-dependent warpage measurement; this is supported by the fact that worldwide installations of temperature-dependent shadow moiré equipment have grown to over 100. Applications include:

- Local-area and global PCB flatness measurement
- Package, IC and wafer flatness measurement
- Lead-free testing
- Part qualification
- Production-level flatness measurement
- QA/QC trending and statistical analysis
- Incoming part inspection

OEMs are also seeing the value of warpage characterization, and several have begun creating their own internal specifications for flatness. In fact, this "OEM push" is the primary driver for the flatness

measurement equipment installations. Examples of current OEM initiatives are listed below:

- Major network equipment company has local-area PCB flatness spec for BGA bond pad sites (maximum coplanarity of 100 micron or 4 mil). Company was able to show a decrease in failure rate from 20-30% to less than 0.5% after implementing this spec.
- Major computer maker has 200-micron (8 mil) spec for PBGAs greater than 30mm square, which is currently used for package qualification and in-line monitoring. This spec is unique in that it specifies a maximum warpage allowable *over the entire reflow profile,* not just at room temperature.
- Asian consumer electronics company is now employing temperature-dependent measurement of Package-on-Package (PoP) on the production floor for QA/QC sampling and lot-to-lot variation/trending. This is the first such implementation of shadow moiré technology.

In May of 2005, JEDEC published the first test method for high-temperature package warpage (JEDEC Standard JESD22B112, "High Temperature Package Warpage Methodology"). This standard not only underscores the importance of flatness on bond integrity and reliability, but also demonstrates the need for warpage measurement during reflow. In other words, a simple "before and after" measurement will not suffice; packages must be characterized – and their mechanical stability confirmed – during the entire reflow profile. This standard specifically cites shadow moiré as a suitable technique for measurement during reflow profiling. JEITA is currently working on a similar standard for package warpage.

SUMMARY

Warpage characterization of packages and PCBs are becoming more critical as geometries become smaller (finer pitches, smaller solder ball volumes, thinner substrates, etc.). Compounding this is the lead-free initiative, which requires higher processing temperatures; these higher temperatures magnify CTE mismatches and generally increase warpage of packages and PCBs. As a result, temperature-dependent warpage characterization is now more important than ever, and the industry has responded to this. JEDEC's new JESD22B112 standard, as well as pending standards from other committees, demonstrate the growing importance of flatness measurement. Perhaps more importantly, OEMs are now leading the way by implementing their own internal initiatives, which are further strengthened now that a standard is in place. As a result, companies are experiencing improvements in yield and reliability, which have begun to filter down through the supply chain.