EFFECT OF PRINTED WIRING BOARD WARPAGE ON BALL GRID ARRAYS OVER TEMPERATURE

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ABSTRACT
A study was undertaken to determine the extent to which a printed wiring board will warp during reflow, and the effect this may have upon ball grid arrays being soldered to the board. One of the goals was to determine if a correlation existed between printed wiring board warp and electrical opens on ball grid arrays.

Key words: BGA, electrical opens, warpage, printed wiring board

BACKGROUND
Several board designs being assembled by Raytheon use back-to-back, mirrored ball grid arrays on a multi-layer printed wiring board (see Figure 1). The ball grid arrays are cavity-down, metal-lidded parts. This type of back-to-back BGA design leads to many assembly and rework challenges. Electrical opens on the ball grid arrays have also been a major issue with these designs. Therefore, a team was put into place to determine why electrical opens were occurring and to make the appropriate design changes to eliminate the opens.

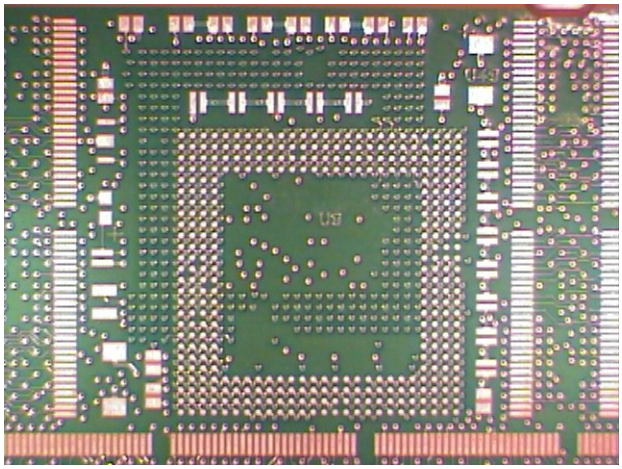

Figure 1: Photograph showing the back-to-back ball grid array pattern on the printed wiring boards.

The opens were identified on various balls on many of the BGA's. There appeared to be no specific pattern as to the location of the failures. The opens could not be detected with x-ray laminography equipment. Therefore, a number of alternate failure analysis techniques were used to locate the cause of the problem. These techniques included scanning electron microscopy, acoustical microscopy, electrical fault isolation and microsectioning. The optimal failure analysis method was found to be microsectioning with a dental burr. The BGA lid was carefully sectioned with the tool until the lid portion of the questionable ball and pad were mechanically isolated. If there was separation at the interconnect, the lid would fall off and the ball and package pad could then be examined to see if the pad itself was loose or if there was cracking through the solder joint. Most of the opens appeared to be the result of cracking at the interface between the BGA package and balls (see Figure 2). Under high magnification, cup and cone on the package pads was apparent. This is indicative of a solder joint tensile stress failure (see Figure 3).

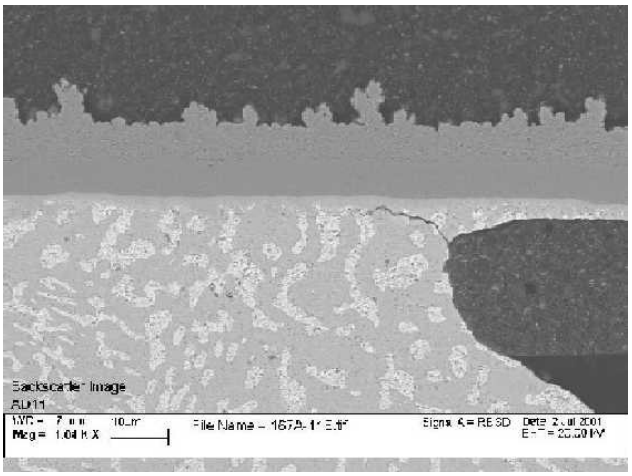

Figure 2: Evidence of cracking can be seen near the interface between the ball and the package.

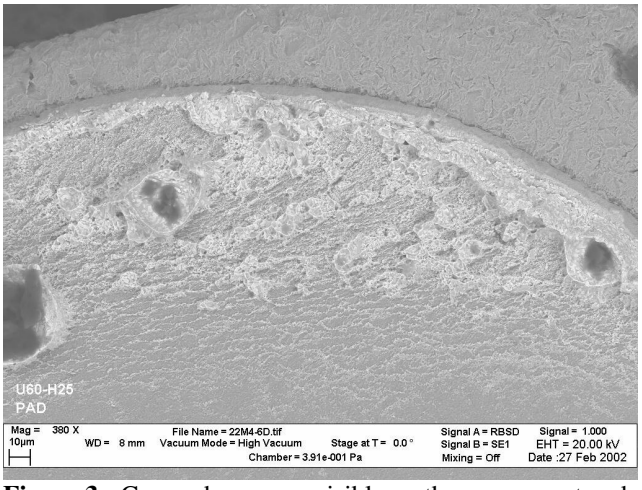

Figure 3: Cup and cone are visible on the component pad surface indicating the application of a tensile stress.

The team then set out to determine what type of tensile stresses could be causing these cracks. A fishbone diagram was done to outline the possible reasons for failure. A summary of these causes can be found in Figure 4. The ball grid array manufacturers were questioned, and no process issues were identified at the component level which would result in a tensile stress failure. A thorough investigation was also done into the circuit card assembly process. Component placement, board reflow, rework and overall handling were all examined and eliminated as possible causes of the failures.

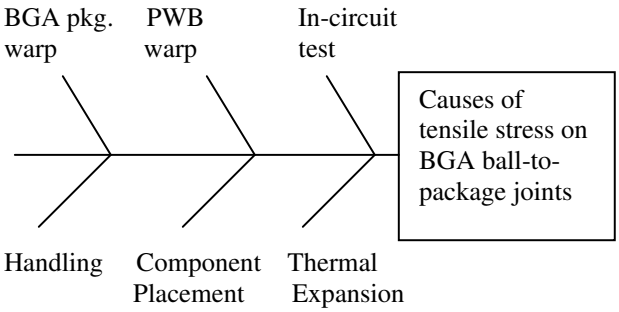

Figure 4: Fishbone diagram of possible sources of tensile stress on the ball-to-package joint.

The printed wiring boards were initially not thought to be suspect because they did not have any indication of flatness problems. The majority of these printed wiring boards did not have a completely balanced construction. However, the PWBs did have a flatness specification of 5 mils per inch on the procurement drawing, and the boards were meeting this requirement. This was attributed to having nine (9) two-ounce copper plane layers and ten (10) signal layers within a nominal .093" thick PWB (see Appendix A). Also, there was no indication that the PWBs were outside of the 5 mils per inch specification at room temperature after assembly. In any case, warp during reflow and at operating temperatures was a possibility since the board was not balanced.

SHADOW MOIRE INTERFEROMETRY

In an effort to evaluate warpage over temperature, a company named Akrometrix was consulted. Akrometrix is located in Atlanta, GA and uses patented testing equipment based upon shadow moire interferometry to determine the extent of curvature on a part or board. The test involves placing a board, BGA or circuit card assembly under a sheet of glass etched with equally-spaced parallel lines. The sample is painted white to allow for better reflection. Therefore, this was considered a destructive test as the samples were not able to be re-introduced into the assembly flow. A beam of white light is projected at a 45-degree angle onto the glass, and the shadow produces a moire fringe pattern if the specimen is curved or warped (see Figure 5). These patterns can be "read" to determine in which direction the warp is occurring, as well as the amount of deflection. Figures 6 and 7 are examples of moire fringe patterns. The major advantage in using Akrometrix's services was their ability to subject the test specimen to thermal excursions and take measurements of warp over temperature.

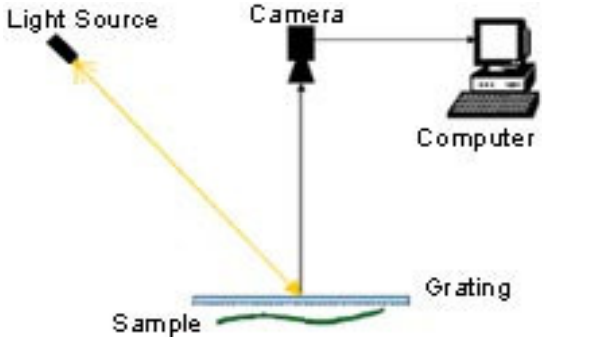

Figure 5: Shadow moiré components.

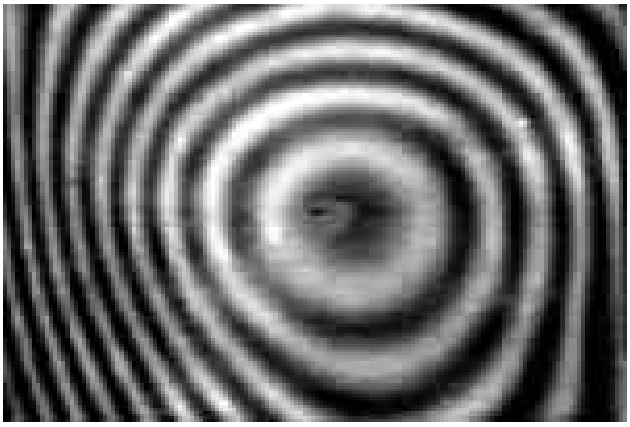

Figure 6: "Bullseye" shadow moiré pattern indicating that the sample is warped in a shape resembling a bowl.

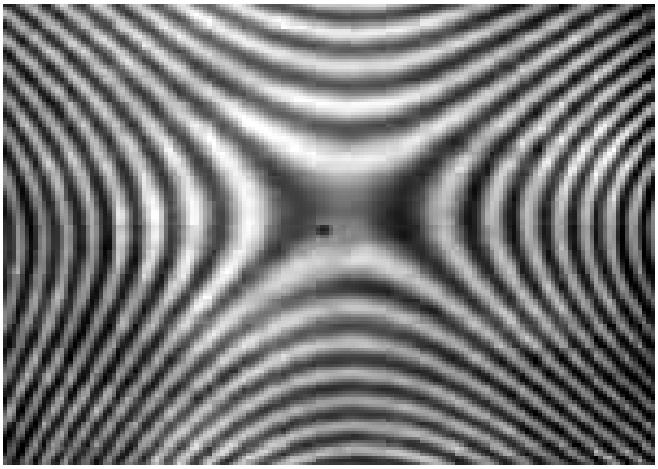

Figure 7: "Saddle-shaped" shadow moiré pattern indicating that the sample is warped in a shape resembling a saddle.

TEST SAMPLES AND METHODOLOGY

Five blank printed wiring boards, seventeen ball grid arrays and one circuit card assembly were taken to Akrometrix for testing.

Printed Wiring Boards

Four of the five PWBs (denoted as PWBs 1 through 4) were all high-temperature epoxy boards with a total of nineteen layers and each with 8-9 two-ounce copper planes. The fifth PWB (denoted as PWB 5) was a sequentially-laminated, Polymer-On-Polymer (POP) board with 20 layers and only 1 oz. versus the 2 oz. copper plane layers on the multi-layer designs. Thus, this board was better balanced than the other four PWB's.

Ball Grid Arrays

Fourteen of the ball grid arrays (denoted as BGAs 1 through 14) were 352 I/O, cavity-down, metal-lidded parts. The remaining three (denoted as BGAs 14 through 17) were 652 I/O, cavity-down SuperBGA-style parts.

Neither the PWBs nor the BGA packages had been subjected to thermal excursions beyond those used to fabricate the boards and assemble the BGAs. These components were tested in the "as-received" condition.

Circuit Card Assembly

The assembled board had five back-to-back, BGAs (10 total) plus one additional BGA. As previously mentioned, the back-to-back BGAs were slightly offset so as not to be completely under each other. The assembly also had four metal heat exchanger bars, two per side, for cooling purposes. These also acted as board stiffeners. This circuit card assembly had gone through two inline reflow excursions during initial assembly, and had been heated during removal of at least one BGA.

All PWBs were moisture baked at 125 degrees celsius for four hours prior to thermal testing. All BGA's and the circuit card assembly were baked at 125 degrees celsius for 24 hours. The exact reflow profiles developed by assembly shop personnel were used to derive the simulation profiles. Warp measurements were taken at the following temperatures: 26 degrees celsius before pre-bake, 26 degrees celsius after pre-bake, 70 degrees celsius upon heating, 130 degrees celsius upon heating, 183 degrees celsius upon heating, peak profile temperature (208 or 213 degrees celsius, depending upon the sample), 183 degrees celsius cooling, 130 degrees celsius cooling, 70 degrees celsius cooling and 26 degrees celsius final room temperature.

TEST RESULTS

Printed Wiring Boards

Coplanarity was a key measurement used to evaluate the magnitude of warp. Akrometrix defines coplanarity as the highest point of deflection minus the lowest point of deflection. Akrometrix also utilizes patented software to generate three-dimensional surface plots and two-dimensional diagonal plots to aid in deciphering the data. Figure 8 is a surface plot of PWB 1 at 130 degrees celsius upon cooling. It shows board deflection in the positive z direction of up to 38.3 mils and deflection in the negative z direction down to –17.0 mils. This gives an overall coplanarity value of 55.3 mils, just outside the specification of 5.53 mils/inch, with the PWBs approximately 10 inches on the diagonal. All four corners of the PWB were warped upward, while the center section was warped downward. The corresponding diagonal plot (Figure 9) shows what is happening along the two diagonals of the board. Positive displacement is seen at the corners, followed by negative displacement toward the center of the board, and then positive displacement again at the opposite corners.

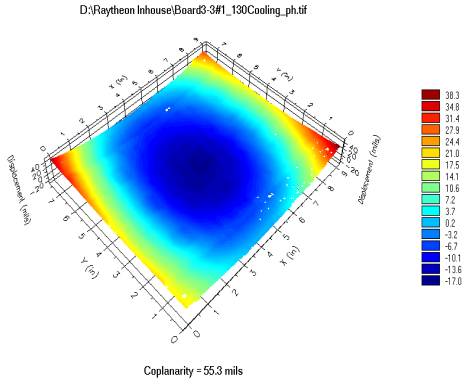

Figure 8: Surface plot of PWB 1 showing warp in the positive direction in all four corners and two sides, and warp in the negative direction in the center section.

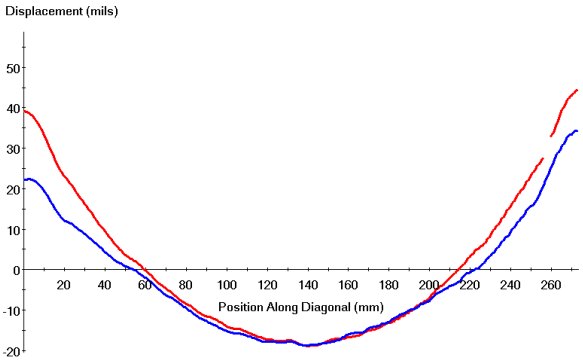

Figure 9 Diagonal plot of PWB 1 showing initial positive displacement in the corners followed by negative displacement, and then positive displacement in the opposing corners.

This coplanarity data was then analyzed to determine the relative change in deflection over temperature along the diagonals of each board. Table 1 gives the maximum diagonal change in deflection over temperature for each printed wiring board sample. A maximum change in deflection was seen to be 7.0 mils per inch while the average change in deflection for the multi-layer high temperature epoxy boards was 4.3 mils per inch. Adding only the average change to the possible room temperature deflection of 5 mils per inch, a total deflection of 9.3 mils or more is quite possible. Even the more balanced, sequentially-laminated board saw 5.1 mils of deflection. This was more than expected, but could be due to the nature of construction. Although designed to be balanced, each

side of the PWB is independent. This change in displacement over temperature is obviously very detrimental to the ball grid array solder joints located on the board.

Sample	Type of Construction	Deflection Due to Temperature Change (mils/in.)
PWB 1	Multilayer High-Temp Epoxy (19 layers)	2.9
PWB 2	Multilayer High-Temp Epoxy (19 layers)	7.0
PWB 3	Multilayer High-Temp Epoxy (19 layers)	2.5
PWB 4	Multilayer High-Temp Epoxy (19 layers)	4.9
Average		4.3
PWB 5	Sequential Lamination/Balanced Construction (20 layers)	5.1

Table 1: Printed wiring board deflection over temperature (mils/inch).

Ball Grid Arrays

The change in deflection over temperature was then calculated for all of the ball grid array samples (see Table 2). The average maximum diagonal change in deflection for the 352-pin ball grid arrays was 1.9 mils and .5 mils for the 652-pin ball grid array. Thus, the larger, 652-pin ball grid array package appeared to warp less than the 352-pin packages. This was a bit surprising since the 652-pin package has a 60% larger surface area.

Circuit Card Assembly

An unbalanced, nineteen-layer PWB with twelve back-to-back BGAs was the foundation of the circuit card assembly. The assembly was tested while undergoing two separate simulated reflow profiles as well as a cold temperature test. The first reflow profile simulation was performed with side "A" up, and the second simulation with side "B" up. Running these two reflow profiles allowed for a better simulation of the actual assembly process, although both sides of the sample circuit card assembly were already populated with components. The cold temperature test allowed measurements to be taken at room temperature, 0, -20, -30 and –40 degrees celsius. The circuit card assembly was placed in the same fixture which is used to assemble the board on the inline equipment. This is a window-pane type fixture with clamps to gently hold the metal heat exchangers in place.

The maximum change in deflection over the entire surface of the circuit card assembly was 4.2 mils per inch during reflow. Measurements were also taken on the board after cooldown outside of the fixture. No significant change in warp was noted; therefore, the fixture did not seem to have an impact on warpage. However, a measurement was taken twelve hours after cooldown, and a 50% reduction in coplanarity was found.

Exposure to cold temperatures did not have a significant impact on board warp. Only .4 mils of deflection were noted over the temperature range. See Table 3 for a summary of the assembled board coplanarity data.

Sample	Number of I/O	Deflection Due to Temperature Change (mils/in.)
BGA 1	352	3.8
BGA 2	352	2.8
BGA 3	352	3.3
BGA 4	352	1.1
BGA 5	352	1.3
BGA 6	352	1.7
BGA 7	352	2.0
BGA 8	352	1.7
BGA 9	352	1.4
BGA 10	352	1.7
BGA 11	352	1.8
BGA 12	352	2.0
BGA 13	352	.8
BGA 14	352	1.2
Average	**352**	**1.9**
BGA 15	652	.5
BGA 16	652	.6
BGA 17	652	.5
Average	**652**	**.5**

Table 2: Ball grid array deflection over temperature (mils/inch).

Sample	Deflection Due to Temperature Change (mils/in.)
Circuit Card Assembly, reflow	4.2
Circuit Card Assembly, cold temperatures	.4

Table 3: Circuit card assembly deflecton over temperature (mils/inch).

CORRECTIVE ACTIONS

Based on the thermal deflections witnessed over temperature, the team determined that the largest contributor to the system deflection was the printed wiring boards. In addition, the team had little design influence over the ball grid arrays and packaging technology. The obvious answer was to modify the printed wiring board layer stack-up so as to balance the construction for the multi-layer PWBs in an effort to minimize the potential for warp.

The team reviewed the 19-layer PWB design. In order to balance the construction of the multi-layer PWBs, inputs

from the PWB supplier(s), mechanical engineering (thermal dissipation), and product development engineering (PWB packaging) were required. Although the PWB thickness of .093" with ten impedance-controlled layers and nine plane layers was constraining, the suppliers(s) used historical data to determine that an additional copper layer could be successfully added to the stack-up while maintaining the overall thickness requirement. Also, the thermal measurements obtained by mechanical engineering allowed for a decrease in the amount of copper required in many of the designs. As a result, product development engineering was able to balance the construction with a combination of 1 oz. and 2 oz. copper planes that maintained thickness, impedance, and thermal dissipation requirements. In addition, all 2 oz. copper plane layers were replaced with 1 oz. copper in some designs. See Appendix A for before and after snapshots of the PWB stack-ups.

The sequentially-laminated PWB exhibited a large degree of deflection upon thermal cycling, but the board was as balanced as possible from a sequential lamination perspective. Each half of the PWB was individually balanced as was the overall PWB. The team did not believe the design could be improved; however, there was risk for inherent variability as those designs were fabricated independently.

SUBSEQUENT TESTING/FOLLOW-UP NOTES

After the board construction was balanced, samples were sent back to Akrometrix for re-testing. Six PWBs were subjected to the same simulated reflow profile which was previously used for testing. The boards were again baked for four hours at 125 degrees celsius, and warp measurements were taken at the same temperatures. The data showed a significant reduction in deflection over temperature on all six PWBs. See Table 4 below for deflection data.

Sample	**Type of Construction**	**Deflection Due to Temperature Change (mils/in.)**
PWB 1	Multilayer High-Temp Epoxy	1.4
PWB 2	Multilayer High-Temp Epoxy	1.6
PWB 3	Multilayer High-Temp Epoxy	3.0
PWB 4	Multilayer High-Temp Epoxy	1.0
PWB 5	Multilayer High-Temp Epoxy	.9
PWB 6	Multilayer High-Temp Epoxy	1.8
Average		**1.6**

Table 4: Re-designed, symmetrical printed wiring board deflection over temperature (mils/inch).

Several hundred boards have now been assembled with the new, balanced printed wiring boards. No BGA electrical opens have been seen which can be attributed to printed wiring board warpage.

CONCLUSIONS

This analysis showed that a correlation between printed wiring board deflection over temperature and BGA electrical opens does exist. PWBs can warp significantly over temperature and can most likely cause cracking at the solder joint interface between the ball and the BGA package. It was proven that printed wiring boards that are flat at room temperature and meet standard flatness specifications may warp over temperature excursions and then return to "normal" at room temperature. Therefore, it is very important that boards have a balanced construction in order to minimize this warp over temperature as much as possible.

ACKNOWLEDGEMENTS

The authors would like to thank fellow BGA Defect Resolution Team members Pete Peterson, John Sanders, Kent Schumacher, Gordon Magnus, Phil Lloyd and Justin McMillan for all of their work in determining the cause of the ball grid array failures and for their inputs on how to re-design the printed wiring boards. Thanks also go to Patrick Hassell, Mark Solomon and Greg Petriccione at Akrometrix for their technical assistance. Robert Champaign, Marlin Downey, Todd Snively, Joe Colangelo and Jodi Roepsch from the Raytheon Failure Analysis Laboratory also provided exceptional support.

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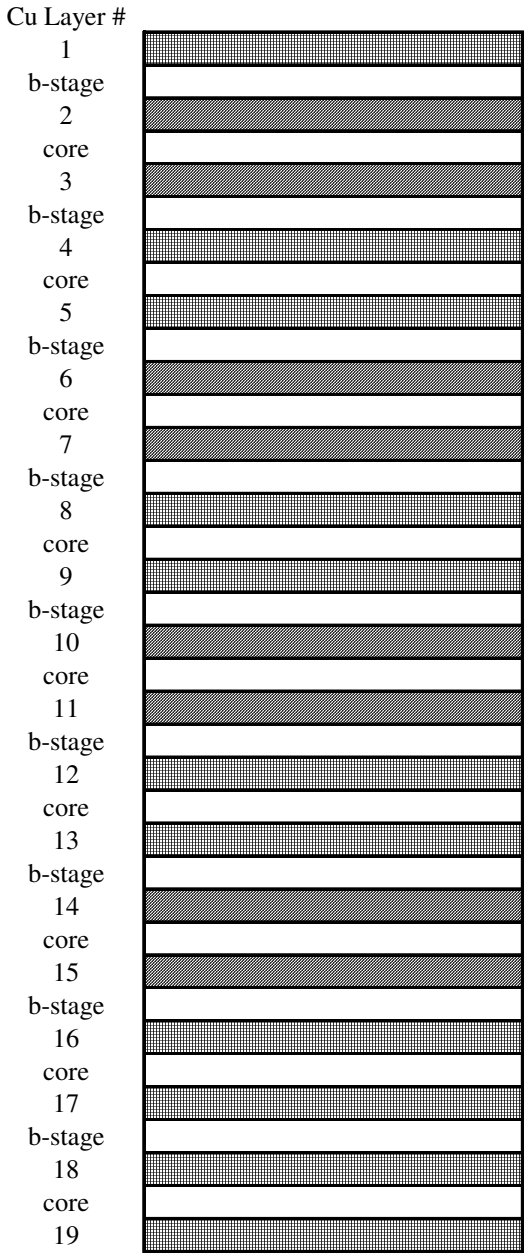
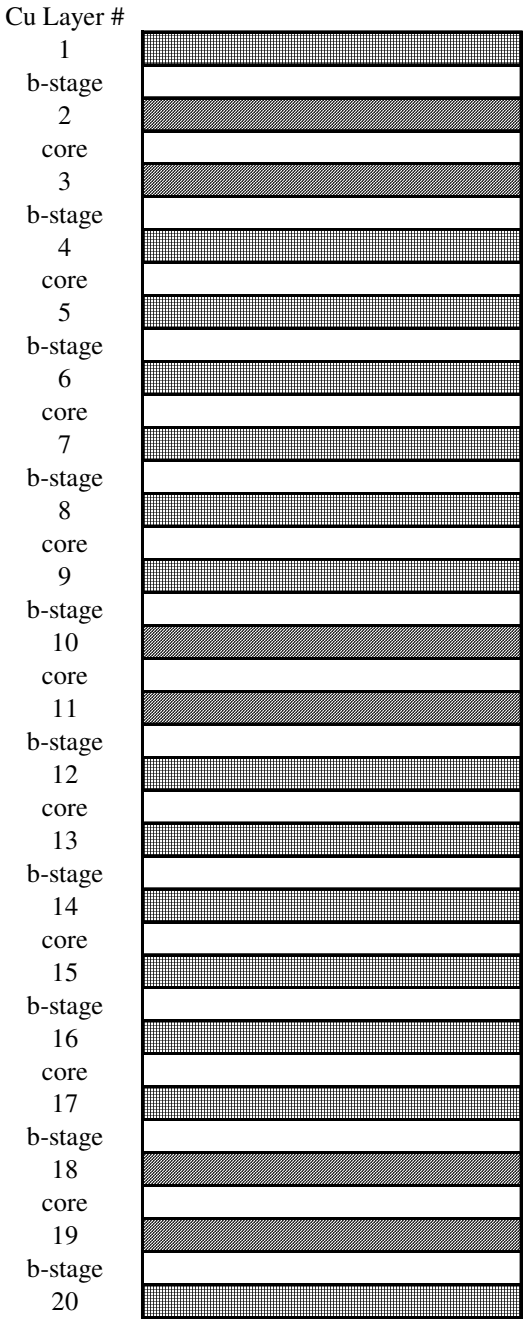
APPENDIX A: COMPARISON OF INITIAL VERSUS BALANCED PWB CONSTRUCTIONS

Initial Construction



PWB - Flat at room temp
CCA - Flat at room temp
.094" thick (nominal)
Wide Coplanarity Variation over temp

Balanced Construction



PWB - Flat at room temp
CCA - Flat at room temp
.094" thick (nominal)
Reduce Coplanarity Variation over temp

LEGEND:

2 oz copper plane layers
b-stage or core dielectric mat'l (high temp epoxy)
1/2 or or 1 oz copper layers