



Bob Willis

Controlling bow and twist

As production problems go, there is one that keeps reoccurring time and time again. As far as the assembler is concerned poor solder paste printing, inconsistent adhesive dispense, misplaced components, and skipped solder joints are a fact of life. How many of these problems can be effected by board flatness? Conventional technology could accommodate bow and twist to a degree, but SMT needs a flat surface from the pads to the resist and the overall board profile. Board suppliers are often criticized, and they in turn blame the designer. The true cause is often unclear with many studies failing to find the root cause.

At the most you may be able to highlight certain design deficiencies. A full review of all the manufacturing process stages—from the start of circuit board fabrication to the final inspection stages in assembly—is the only way you can find that true cause.

One of the key engineering considerations to bear in mind is the glass transition temperature of the basic

material. For example, a traditional FR4 glass epoxy laminate has a glass transition temperature between 115° and 135°C. If during the processing stages this temperature is exceeded, the material changes its state and becomes pliable. And when the temperature drops the board becomes rigid again. In recent years some attention has been paid to the use of high-stability materials, but they cost more.

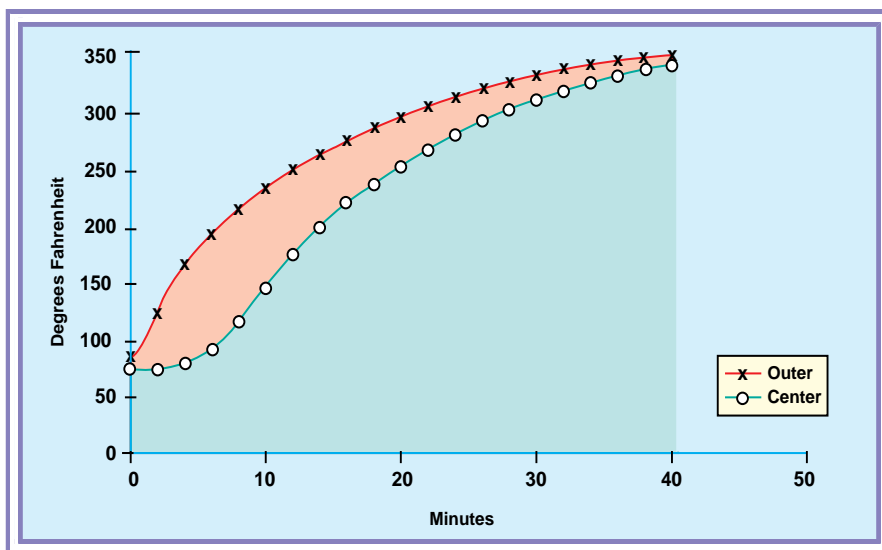
Board stress

There are a number of process stages that may affect the board, both during the manufacture and assembly operations. If stress is present in the board prior to the heating operation, it often results in board warpage. If on the other hand, the board or assembly is not supported correctly during the heating and cooling cycle, the board will have less stress built into the material. As a design engineer you should always aim to layout a construction of a two-layer circuit with copper tracking and earth planes balanced from one side to the other.

The same is also true of a multilayer board, where the internal construction also needs to be balanced. If you have a large copper area on one side of a circuit, it will expand and contract during heating. If the second side has a limited copper coverage, the forces acting on the laminate will be less. You must have seen single-sided boards getting warped particularly when heavy copper is specified.

Effects of component placement

The same can be said for component placement. Unevenly distributed component layout should be considered as weight placed unevenly on the circuit board—it will



The outer boards act as thermal lagging for the rest of the "book". The difference in heat rise rate from the outside to the center causes the resin to gel on the outer side, while the side toward the center remains flowable. The resulting top-to-bottom stresses cause warpage.

inevitably leave stress in the circuit during the cooling stages after soldering. Large connectors and sockets can also restrict board expansion and contraction, leaving a permanent deflection.

The board profile for the final circuit can affect the stress pattern in the material, but the final support during soldering can be a problem, causing stress to be introduced during soldering. Internal profiles and cut outs not only make soldering difficult, but can cause an uneven board surface. All the break-off sections should have copper layers as this makes the board far more rigid for assembly. As the copper is present to start with, it does not add to the cost. Maximizing copper coverage on waste areas is a method often used to support flexible circuits during production.

The circuit manufacturer should consider the basic laminate he is using and perform tests in its basic state regularly and after etching. The number of glass layers in the laminate and prepreg should be maximized as this provides better dimensional stability to the final assembly. Storage and incorrect cutting of the copper-clad laminate can develop defects in the panel. Baking of boards for resist curing or ink drying can cause problems if the panels are not correctly supported and are allowed to sag.

In a typical multilayer lamination process, several multilayer boards are assembled in a stack. Lamination consists of heating this "book" of boards under pressure. Poor control of lamination pressure and high-temperature variations across the process stack (**figure**) build in stress that is only detected at the next high temperature excursion.

Reflow of tin/lead coatings or solder leveling raises the board above the glass transition temperature and may cause the board to warp. The dimensional changes are not always noted at this stage due to the size of the process panel. They come to attention only when the boards are profiled. The fast cooling during washing of flux from the board surface after leveling or reflow is also an issue—the tendency to use cold water rather than hot water in the first washing operation owing to lower cost is a potential cause of thermal shock for the panel.

Provide support against warpage

The circuit assembler subjects the board to temperatures well above the glass transition temperature of most laminates. Wave soldering may be conducted between 235° and 255°C, whereas reflow soldering may subject the board to temperatures in the 215°-to-225°C range. If boards are inadequately supported during the soldering process due to incorrect jiggging, they will be left with a permanent warp or twist.

Have your operating staff set fingers or pin-edge conveyor systems used on wave or reflow soldering such that they allow for board expansion. Boards always expand as they pass through pre-heat and up to soldering temperature. If the jig used to support boards in mass soldering is incorrectly designed, it may securely hold the boards without allowing for expansion. This can be worse than soldering without support.

Baking boards

Assembly companies are often required to bake poor quality boards to overcome outgassing. This can add to distortion if high temperature or poor oven loading procedures are used.

Current test methods are documented in British Standards and IPC specifications. You may get further information either from Preben Lund's handbook "Quality Assessment of Printed Circuit Boards", or on a video tape from IPC.

The test method, which is most often used, requires the board to be placed on a flat surface with the concave side down. A measurement is then taken of the maximum out-of-flatness condition.

Remember, the ultimate flatness of a board can be affected by many factors. It is important to understand that material and board manufacturers, designers, and assembly staff can all affect the quality of the final product. Once this is clear to all parties, the usual "buck passing" will stop. AEE

Causes of warpage span across manufacture, circuit design, and assembly

Although great strides have been made in assembly techniques and board fabrication processes, we are still using basic board materials which turn into a limp "Kleenex" whenever we subject them to heat. Factors that affect board flatness are:

- Laminate material and construction
- PCB outline
- Copper foil and plating thickness
- Even design and circuit layout
- Circuit board fabrication
- Packaging and storage
- Assembly baking cycle
- Soldering operations

Bob Willis is an independent process consultant. Further process advice and information is available at <http://www.bobwillis.co.uk>. You may also e-mail him at eps@bobwillis.co.uk or fax +44-1245-496123.