Survey of Circuit Board Warpage During Reflow

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Goal: Understand typical warpage characteristics of ECM Circuit Board during production solder reflow process

Measurement Methodology
- Tool: Akrometrix Thermal Shadow Moiré Interferometer PS400
  - Simulate production reflow profile
  - IR Heating from bottom side of device being measured
  - Requires step height changes to be less than 0.010” for continuity of measurement
- Board Asm / Substrate lightly coated with white paint to minimize contrast variation

Results
- The board assembly is too dense to get a meaningful measurement of board warpage
  - Not possible to find a straight line across any part of board without crossing a component
  - Step height changes are typically greater than 0.010” causing “computational artifacts”
- Analysis Refocused on unpopulated Circuit Boards
  Results are summarized for various conditions
2007 Engine Control Module Board Assembly

TC 1 (Btm)
TC 2 (Top)
TC 3
Typical Reflow Profile

Part: Asm 09
Profile: Mfg Best Pract SnPb_in.txt

Process 1 = TC Bottom of Board
Process 2 = TC Top of Board
Process 3 = TC Top of PBGA

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Computational Artifacts due to “large” step changes in component heights

Coplanarity = 1322 microns
◆ FR-4, type E67 Circuit Board
  – 1.2 mm (0.047”) thick 6 layer Plated-Thru-Hole
  – 120 mm x 100 mm
  – ENiAu Pad Finish

Board suspended on notched rail each end
Screening Assessment – 3 Boards
Board Warpage vs Reflow Temperature

Board Warpage vs Reflow Temperature
Warpage = Max - Min

Estimated value, due to Computational artifact
Board K Surface Profile During Reflow

27 °C
Board_K_0813(27C)_Board_ph.h
Coplanarity = 277 microns

117 °C
Board_K_0812(117C)_Board_ph.h
Coplanarity = 476 microns

147 °C
Board_K_0818(147C)_Board_ph.h
Coplanarity = 536 microns

180 °C
Board_K_0856(208C)_Board_ph.h
Coplanarity = 518 microns

208 °C
Board_K_0856(208C)_Board_ph.h
Coplanarity = 675 microns

224 °C
Board_K_0321(224C)_Board_ph.h
Coplanarity = 809 microns

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PBGA Pad Area Warpage vs Reflow Temperature

PBGA Area Warpage During Reflow

![Graph showing PBGA area warpage during reflow with different temperatures for Board K, Board L, and Board M.](image-url)
Board K PBGA Pad Area Warpage During Reflow

27 °C

117 °C

147 °C

180 °C

208 °C

224 °C

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Initial Assessment Based on 3 Circuit Boards

- Warpage of Circuit Board
  - Warpage is Significant
  - Variation is Large
  - Changes Run to Run (Gets Worse with Subsequent Runs)

![Warpage vs Reflow Run](chart)

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Sampling Methodology

◆ Circuit Boards were Sampled from Production
  – 7 Different days (Nov 29 thru Jan 19, 2007)
  – Taken directly off of Loader for Screen Printer
  – 9 Boards pulled sequentially from input stack

◆ Boards were lightly coated with high temperature white paint
  – Rustoleum: White - High Heat Paint
  – Air dried 5 minutes
  – Oven dried 10 minutes @ 85 °C

◆ 3 Boards were run within 1 hour of production sampling

◆ 3 Boards were baked dry: 24 hours @ 125 °C

◆ 3 Boards were moisture soaked for 168 hours
  – Time is MSL Level 3 maximum condition for IC packages
  – 4 Groups at 26 °C / 75% RH (Manufacturing Required Practices for Facilities worst case)
  – 3 Groups at 30 °C / 60% RH (J-STD-033B MSL Handling Requirements for IC Packages)
- Boards were subjected to Nominal Mfg Best Practices SnPb Reflow Profile
- Warpage measured / calculated at 13 temperatures
- Data for PBGA Pad Area was adjusted by 22 microns
  - Remove variation due to topology from solder resist / marking
  - Inherent measurement noise
  - Consistent with standard PBGA warpage analysis methodology
Board Warpage vs Reflow Temperature

(Sampled Directly from Production - 24 Bds from 8 lots)
Adjusted Warpage of PBGA Pad Area During Reflow
Sampled Directly from Production - 24 Bds from 8 Lots

Warpage (microns)

Reflow Temperature (C)
Circuit Boards Baked Dry

Circuit Board Warpage - Baked Dry

21 Bds from 7 Lots

Warpage (microns) vs. Reflow Temperature (°C)

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Adjusted Coplanarity of PBGA Pads - Baked Dry

21 Boards from 7 Lots

Reflow Temperature vs. Warpage (microns)
Circuit Board Warpage vs Reflow Temperature

After 168 hrs at 26C/75% RH or 30C/60% RH

Warpage (microns)

Reflow Temperature

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PBGA Bd Area – Wet Condition

Adjusted Warpage of PBGA Area of Board

After 168 hrs at 26 C/75% RH or 30C/60% RH

Warpage (microns)

Reflow Temperature
Multi-Variate Summary of Board Warpage

Warpage of Circuit Board versus Moisture Conditioning
3 Samples per Condition

Data
- Max of Warpage
- Average of Warpage
- Min of Warpage
Multi-Variate Summary of PBGA Area Warpage

PBGA Area of Board vs Moisture Conditioning

3 Samples each Condition

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Statistical Prediction of 30 mm sq PBGA Area Board Warpage - SnPb Reflow Profile

Reflow Temperature (°C) vs. Warpage (microns)

- Solder above Liquidus
- Bd+4.5 Stdev
- Bd+3 Stdev
- Bd Avg
- Bd Data Min
- Bd Data Max
- +0.7% Spec
- -0.7% Spec
- +0.5% Spec
- -0.5% Spec

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Conclusions of Circuit Board Warpage Analysis

- Warpage Varies Significantly by
  - Lot
  - Board
  - Moisture Content
  - Reflow Pass (Starting in Production Condition)

- Effect of Moisture Content Is Not Consistent
  - Effect is Significant within a Lot
  - Optimal Condition Varies by Lot, but generally baked dry is worse

- Warpage of PBGA Area is Large Enough to Impact PBGA Assembly Yields of Large BGAs

- Pb-Free Reflow profiles will cause more warpage

- This study was only single part number / single supplier
Future Work

- Develop Standardized Characterization Methodology
  - Sampling Methodology
    - Random versus Panel / Position
    - # Lots
    - # Samples per Lot
  - Moisture Conditioning? Conditions
  - Characterization Temperatures

- Characterize Additional Part Numbers

- Characterize Pb-Free Reflow Profile

- Determine Acceptable Warpage Specifications
  - Solder Reflow Assembly Process Capability
    - SnPb
    - SAC
  - Allocate Total Warpage Allowance Between Board and BGA
    - Optimize Board Cost / Supply / Industry Standards
    - BGA Cost / Supply / Industry Standards