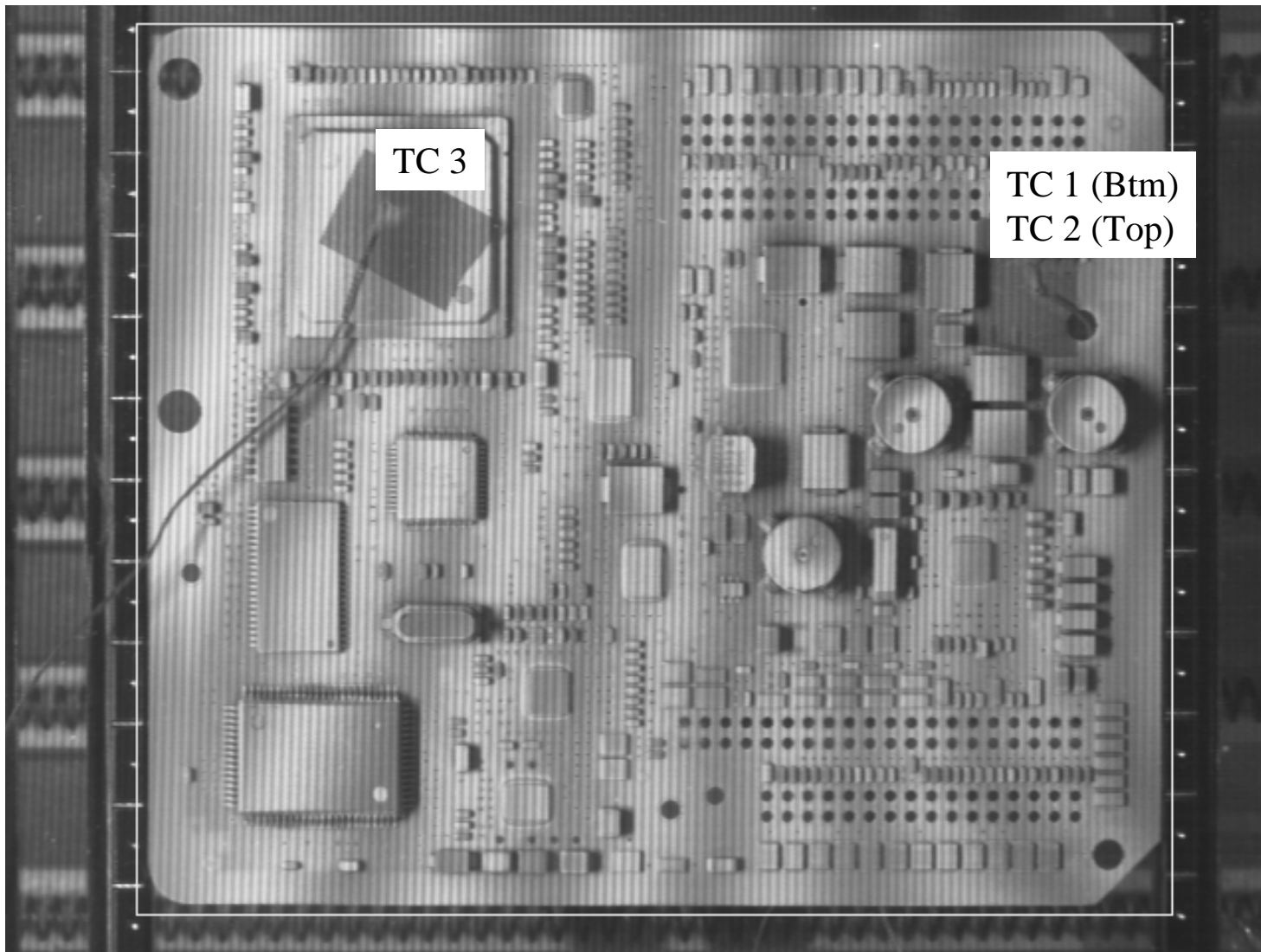


Survey of Circuit Board Warpage During Reflow

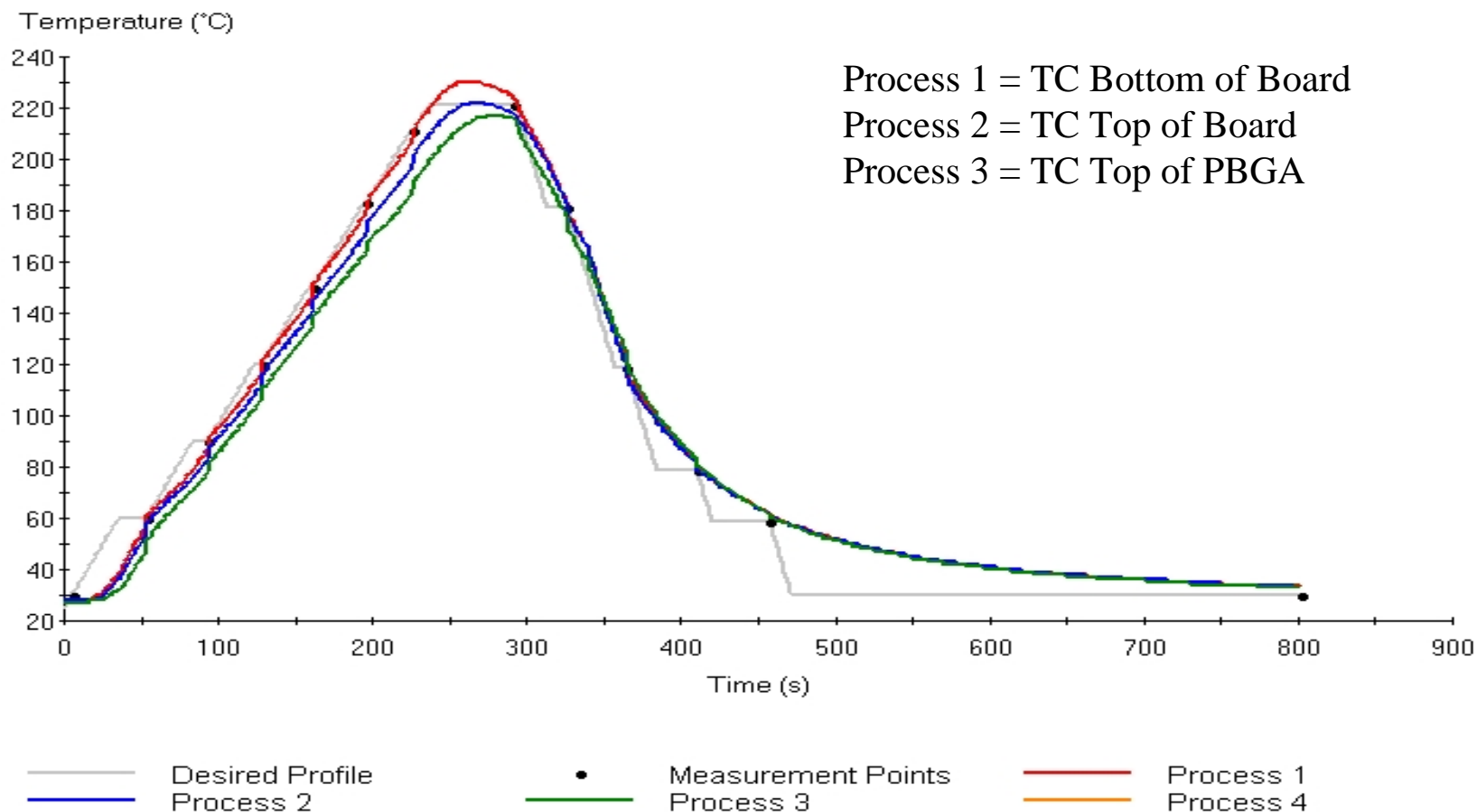
Michael J. Varnau
Delphi Electronics & Safety
8/20/07

- ◆ Overview of Goals & Objectives
- ◆ Overview of Product
- ◆ Initial Circuit Board Characterization (Screening Experiment)
- ◆ Detailed Circuit Board Characterization
 - Sampling / Conditioning Methodology
 - Warpage by Condition
 - » Whole Board
 - » PBGA only Area (30 mm square)
 - Multivariate Analysis: Temperature / Lot / Condition
 - » Whole Board
 - » PBGA only Area
- ◆ Statistical Prediction of Warpage
- ◆ Conclusions – Future Directions

- ◆ Goal: Understand typical warpage characteristics of ECM Circuit Board during production solder reflow process
- ◆ Measurement Methodology
 - Tool: Akrometrix Thermal Shadow Moiré Interferometer PS400
<http://warpfinder.com/shadow-moire.htm>
 - » Simulate production reflow profile
 - » IR Heating from bottom side of device being measured
 - » Requires step height changes to be less than 0.010" for continuity of measurement
 - Board Asm / Substrate lightly coated with white paint to minimize contrast variation
- ◆ Results
 - The board assembly is too dense to get a meaningful measurement of board warpage
 - » Not possible to find a straight line across any part of board without crossing a component
 - » Step height changes are typically greater than 0.010" causing "computational artifacts"
 - Analysis Refocused on unpopulated Circuit Boards
Results are summarized for various conditions



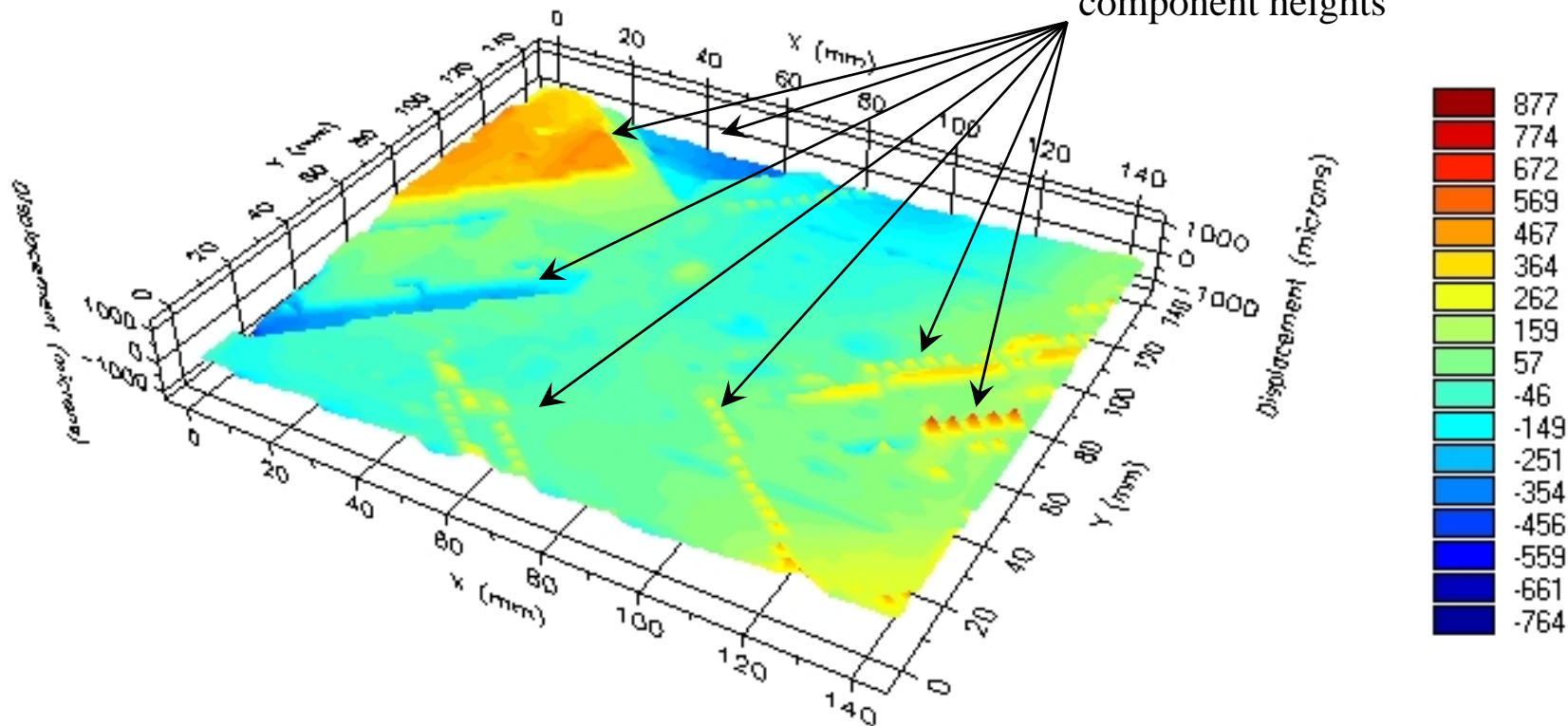
Part: Asm 09
Profile: Mfg Best Pract SnPb_in.bt



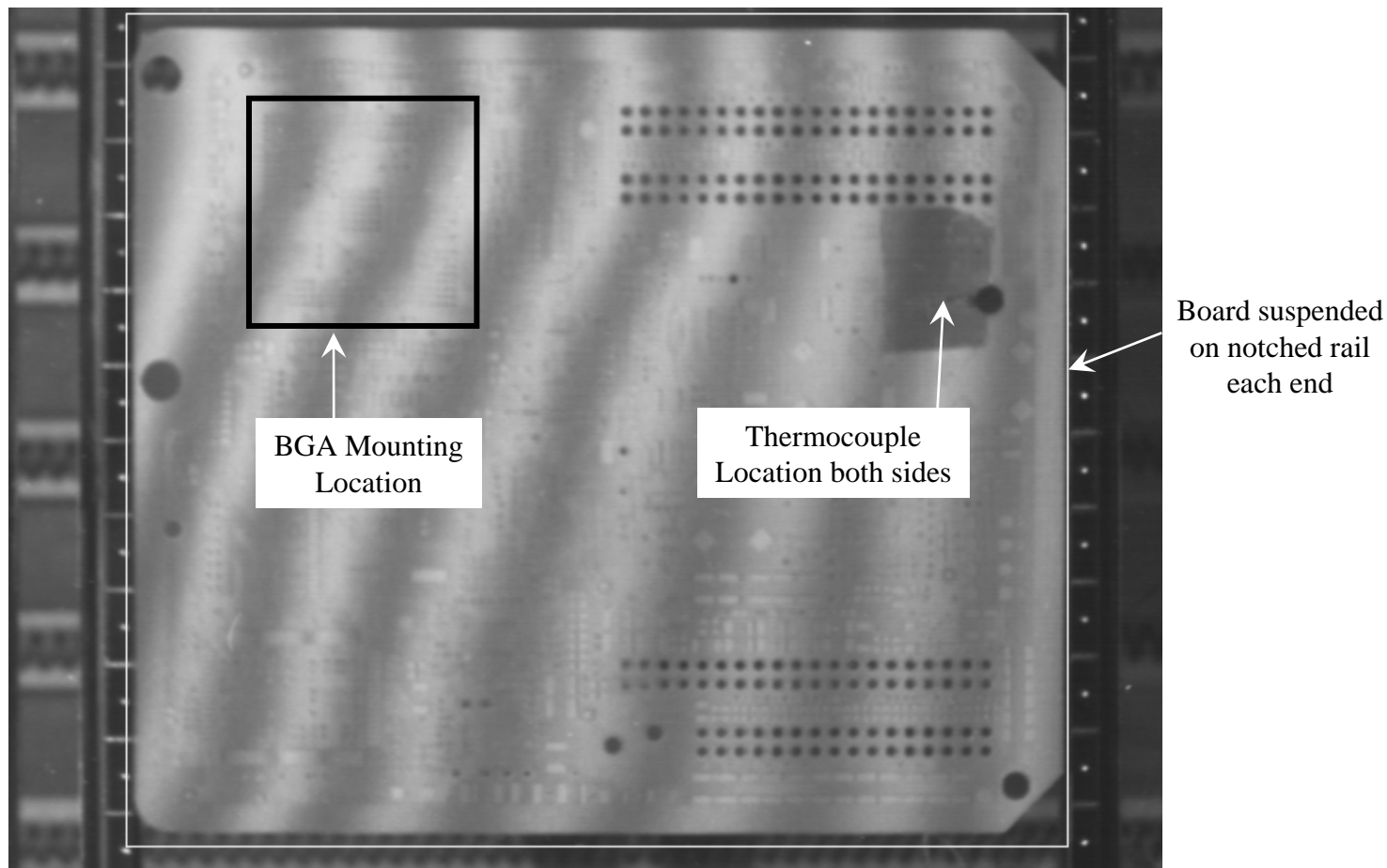
3 D Surface Plot of Board Assembly at 30 °C

Asm 1D_0007(27C)_ph.tif

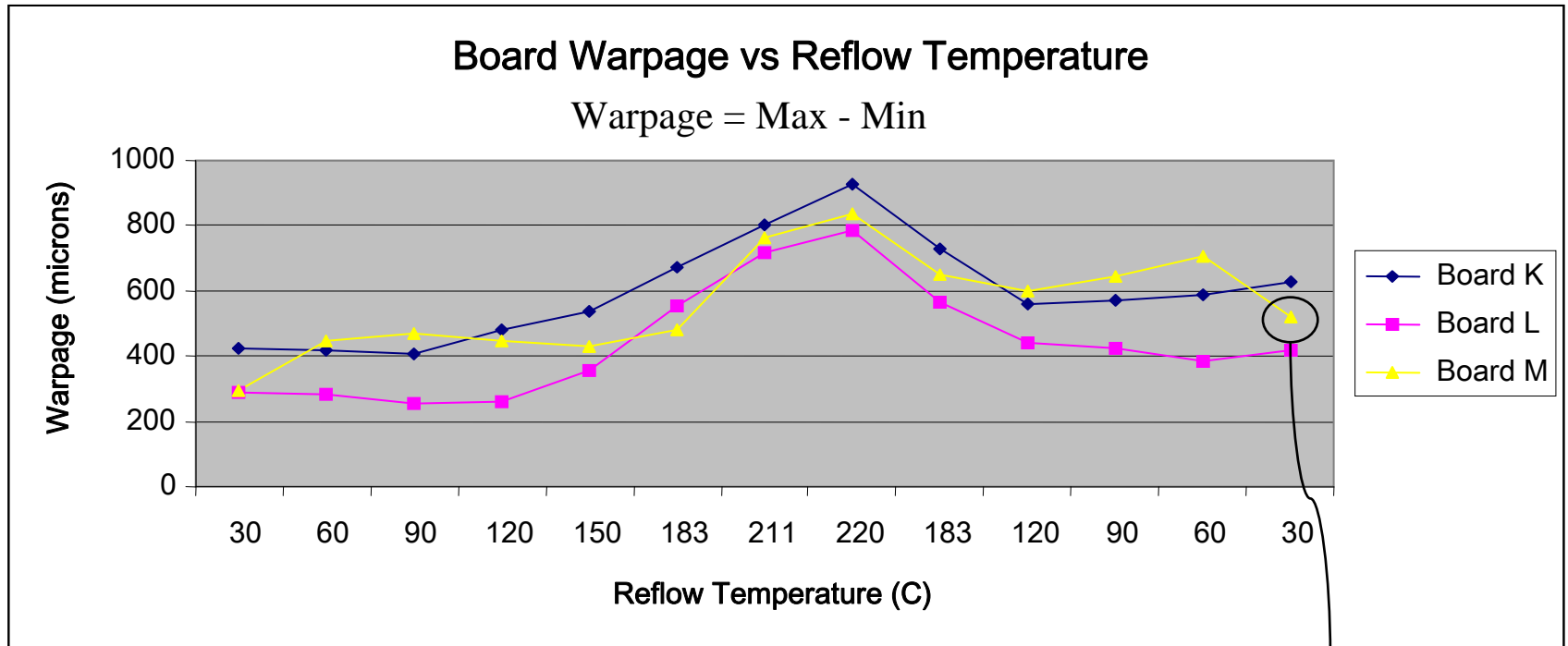
Computational Artifacts due to “large” step changes in component heights



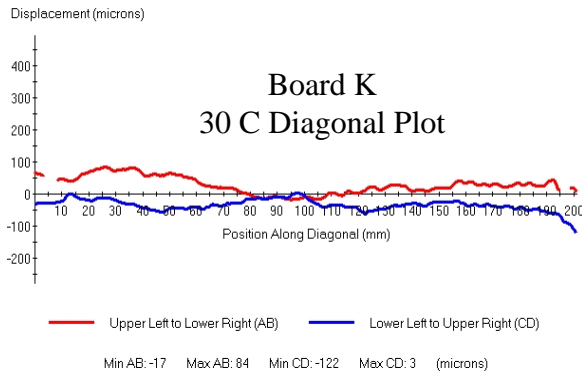
Coplanarity = 1322 microns



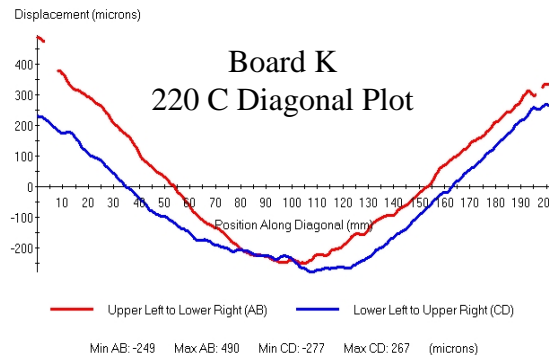
- ◆ FR-4, type E67 Circuit Board
 - 1.2 mm (0.047”) thick 6 layer Plated-Thru-Hole
 - 120 mm x 100 mm
 - ENiAu Pad Finish



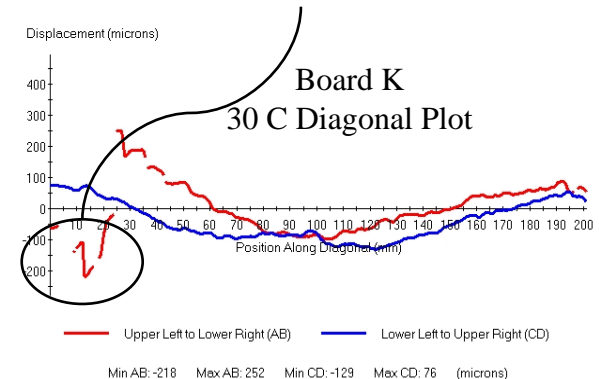
Board M_0005(29C)_Boarad_ph.tif



Board M_0285(220C)_Boarad_ph.tif



Estimated value, due to
Computational artifact

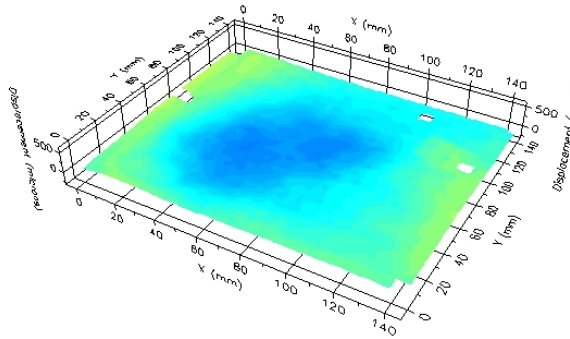


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Board K Surface Profile During Reflow

27 °C

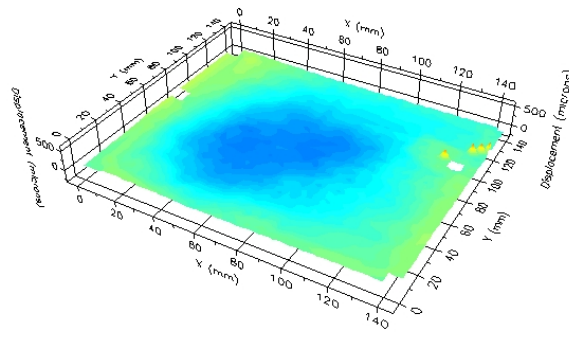
Board K_0035(27C)_Board_ph.tif



Coplanarity = 277 microns

117 °C

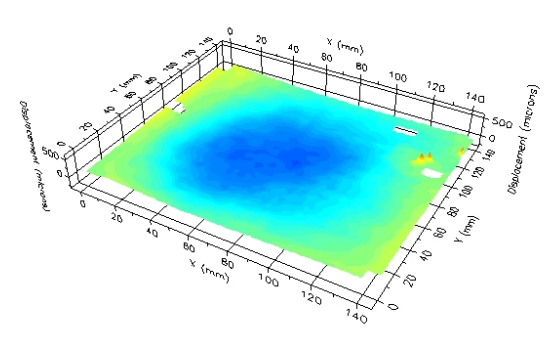
Board K_0150(117C)_Board_ph.tif



Coplanarity = 478 microns

147 °C

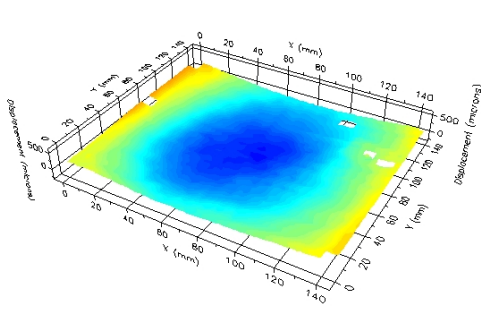
Board K_0186(147C)_Board_ph.tif



Coplanarity = 536 microns

180 °C

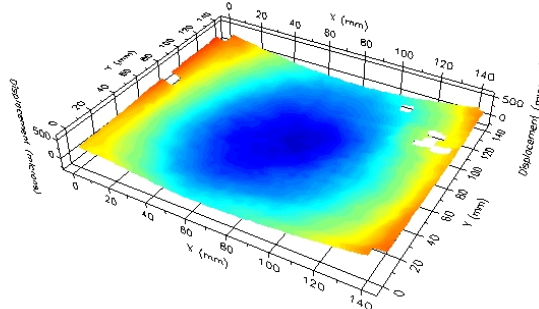
Board K_0225(180C)_Board_ph.tif



Coplanarity = 519 microns

208 °C

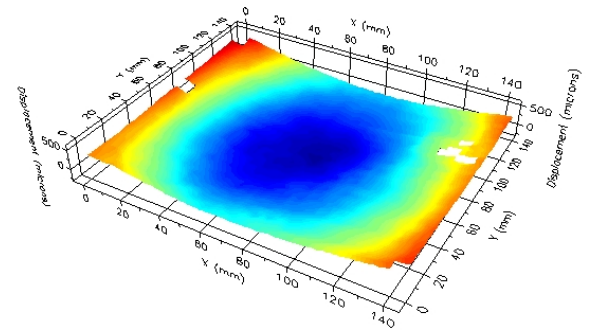
Board K_0258(208C)_Board_ph.tif



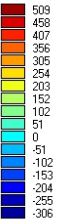
Coplanarity = 675 microns

224 °C

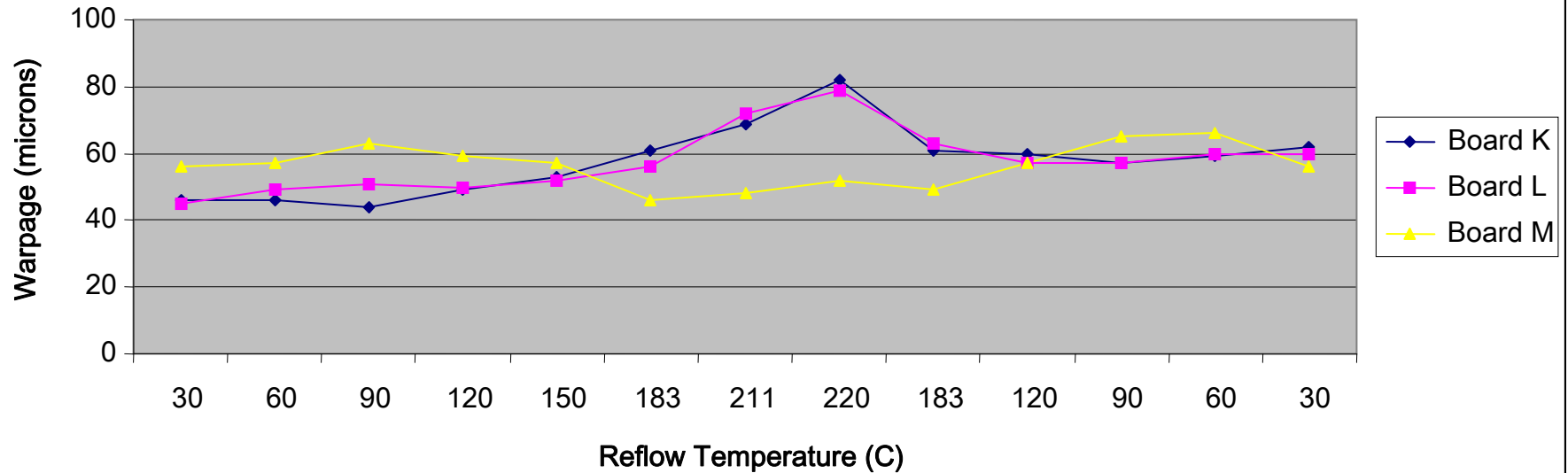
Board K_0321(224C)_Board_ph.tif



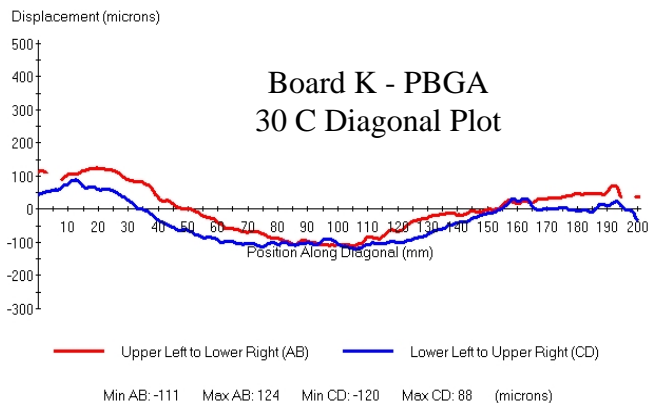
Coplanarity = 809 microns



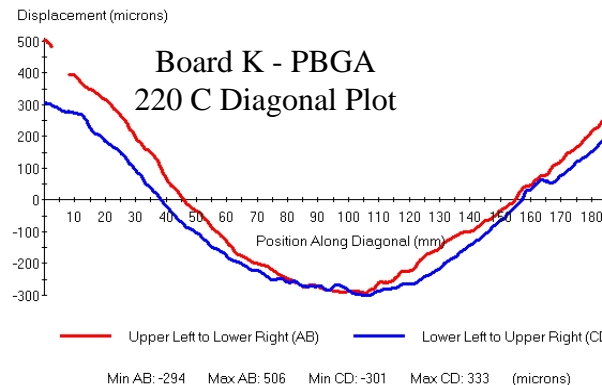
PBGA Area Warpage During Reflow



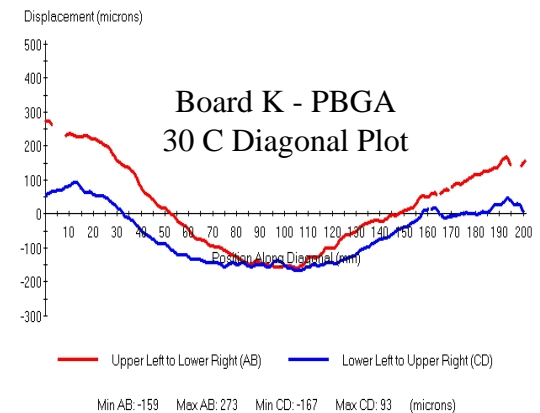
Board K_0035(27C)_Board_ph.tif



Board K_0321(224C)_Board_ph.tif



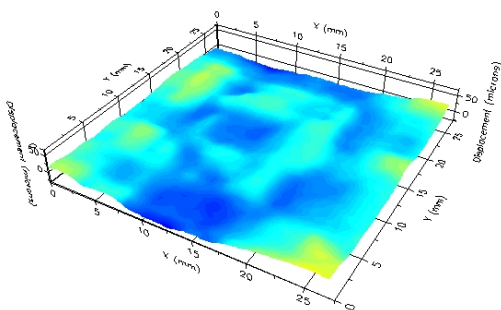
Board K_0759(33C)_Board_ph.tif



Board K PBGA Pad Area Warpage During Reflow

27 °C

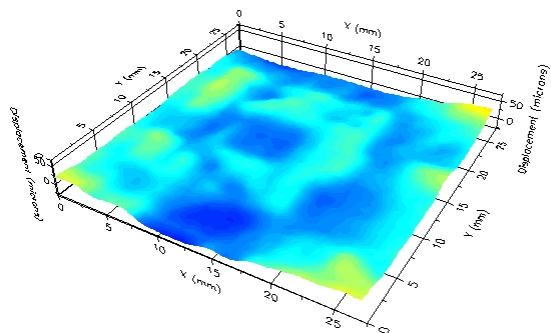
Board K_0035(27C)_BGA Pad Area_ph.tif



Coplanarity = 46 microns

117 °C

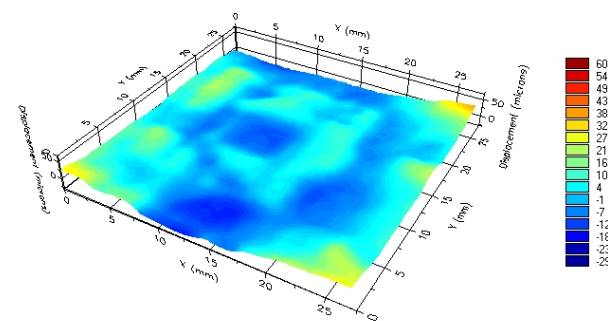
Board K_0150(117C)_BGA Pad Area_ph.tif



Coplanarity = 49 microns

147 °C

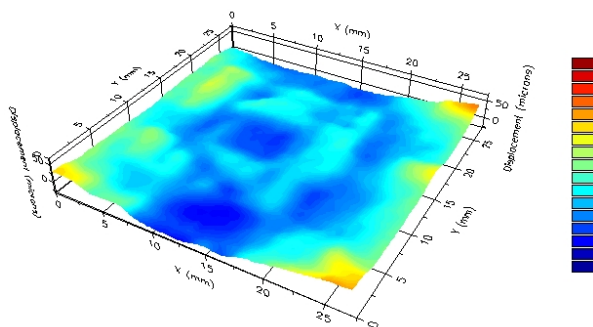
Board K_0186(147C)_BGA Pad Area_ph.tif



Coplanarity = 53 microns

180 °C

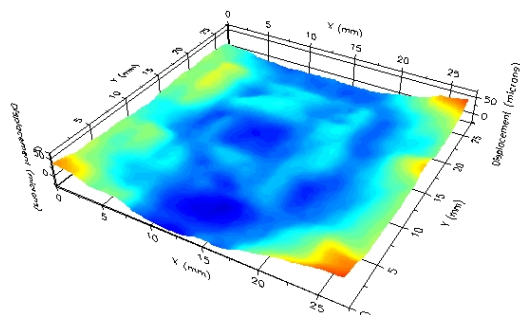
Board K_0225(180C)_BGA Pad Area_ph.tif



Coplanarity = 61 microns

208 °C

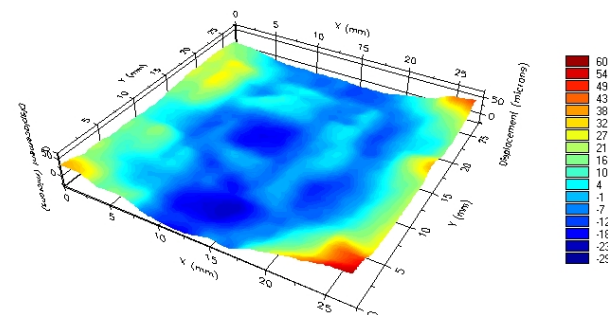
Board K_0258(208C)_BGA Pad Area_ph.tif



Coplanarity = 69 microns

224 °C

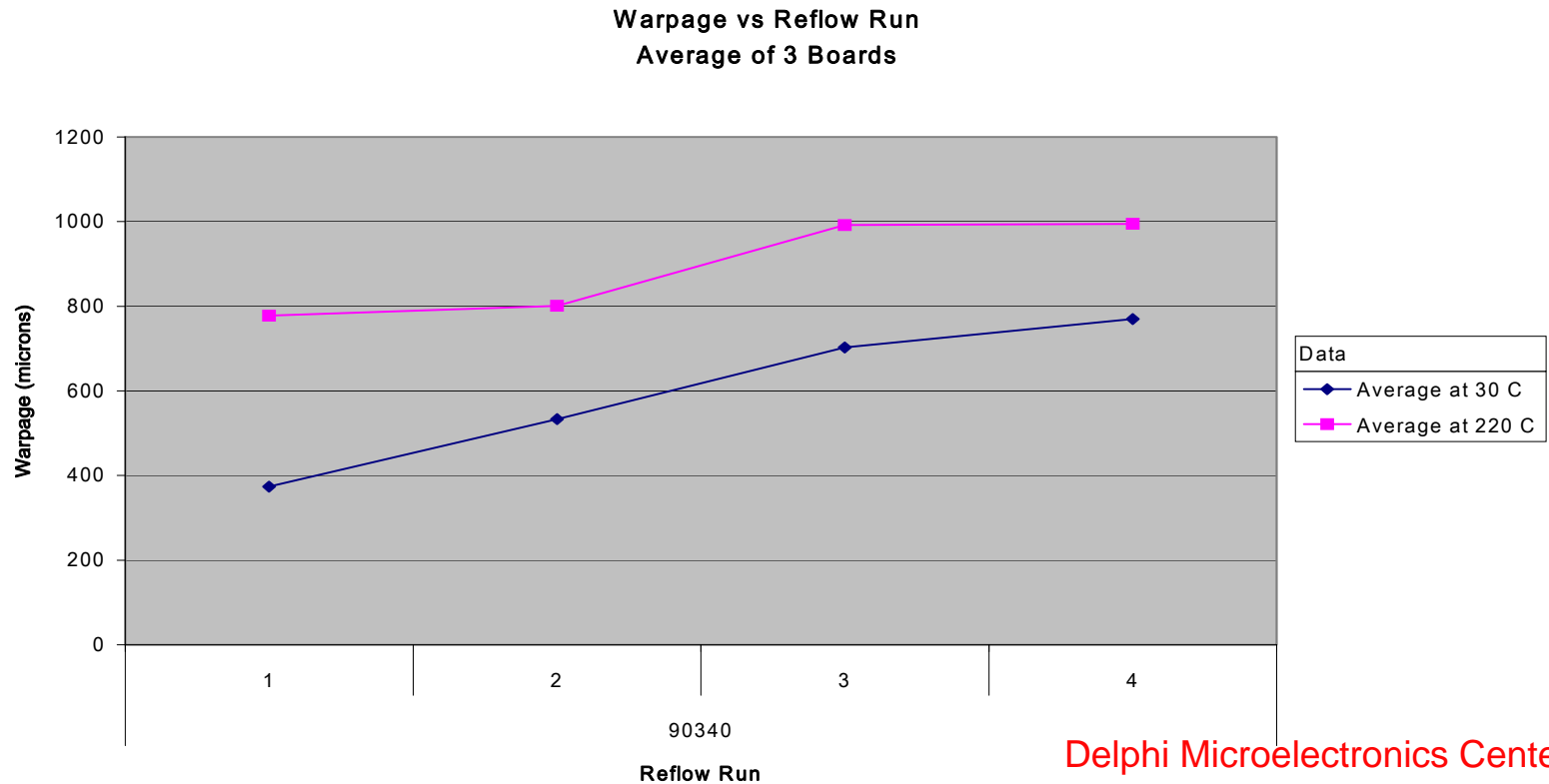
Board K_0321(224C)_BGA Pad Area_ph.tif



Coplanarity = 82 microns

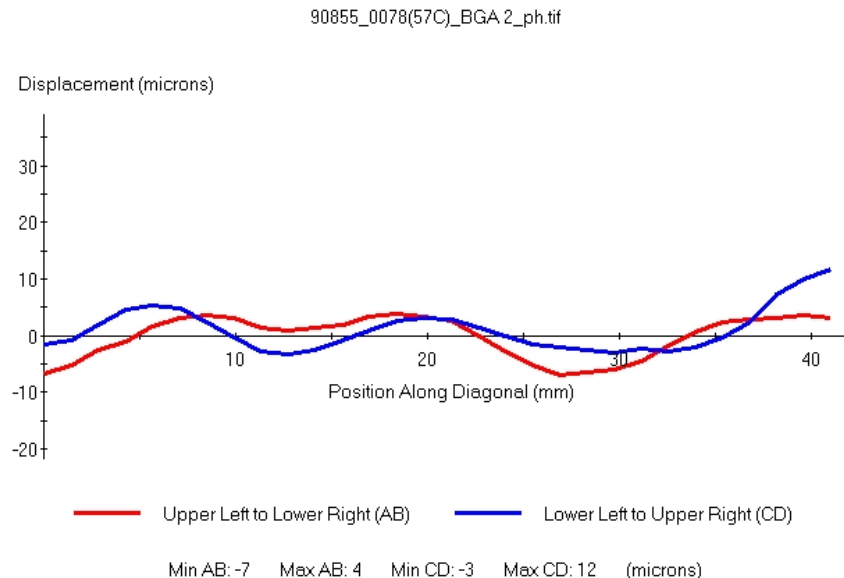
◆ Warpage of Circuit Board

- Warpage is Significant
- Variation is Large
- Changes Run to Run (Gets Worse with Subsequent Runs)

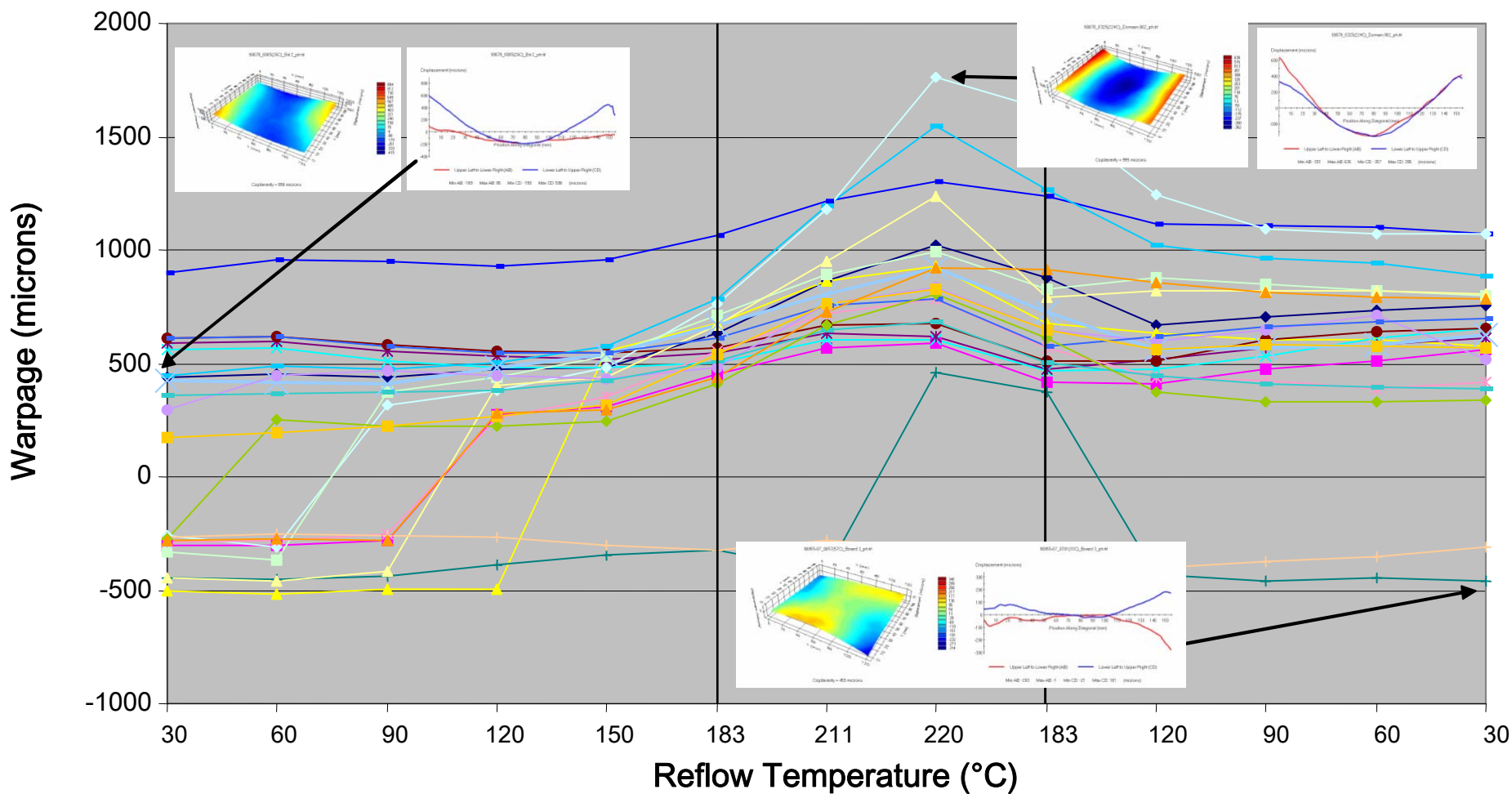


- ◆ Circuit Boards were Sampled from Production
 - 7 Different days (Nov 29 thru Jan 19, 2007)
 - Taken directly off of Loader for Screen Printer
 - 9 Boards pulled sequentially from input stack
- ◆ Boards were lightly coated with high temperature white paint
 - Rustoleum: White - High Heat Paint
 - Air dried 5 minutes
 - Oven dried 10 minutes @ 85 °C
- ◆ 3 Boards were run within 1 hour of production sampling
- ◆ 3 Boards were baked dry: 24 hours @ 125 °C
- ◆ 3 Boards were moisture soaked for 168 hours
 - Time is MSL Level 3 maximum condition for IC packages
 - 4 Groups at 26 °C / 75% RH (Manufacturing Required Practices for Facilities worst case)
 - 3 Groups at 30 °C /60% RH (J-STD-033B MSL Handling Requirements for IC Packages)

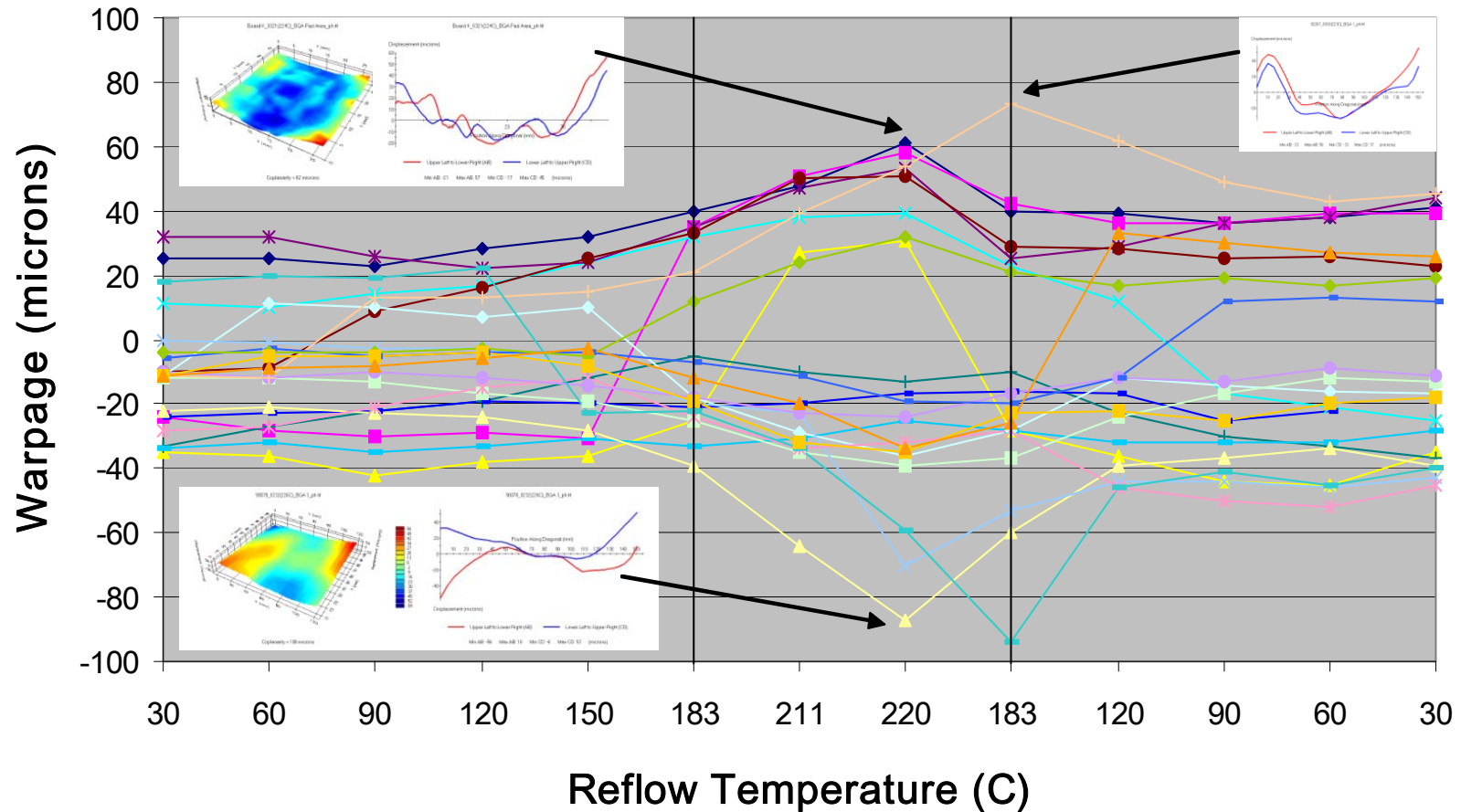
- ◆ Boards were subjected to Nominal Mfg Best Practices SnPb Reflow Profile
- ◆ Warpage measured / calculated at 13 temperatures
- ◆ Data for PBGA Pad Area was adjusted by 22 microns
 - Remove variation due to topology from solder resist / marking
 - Inherent measurement noise
 - Consistent with standard PBGA warpage analysis methodology



(Sampled Directly from Production - 24 Bds from 8 lots)

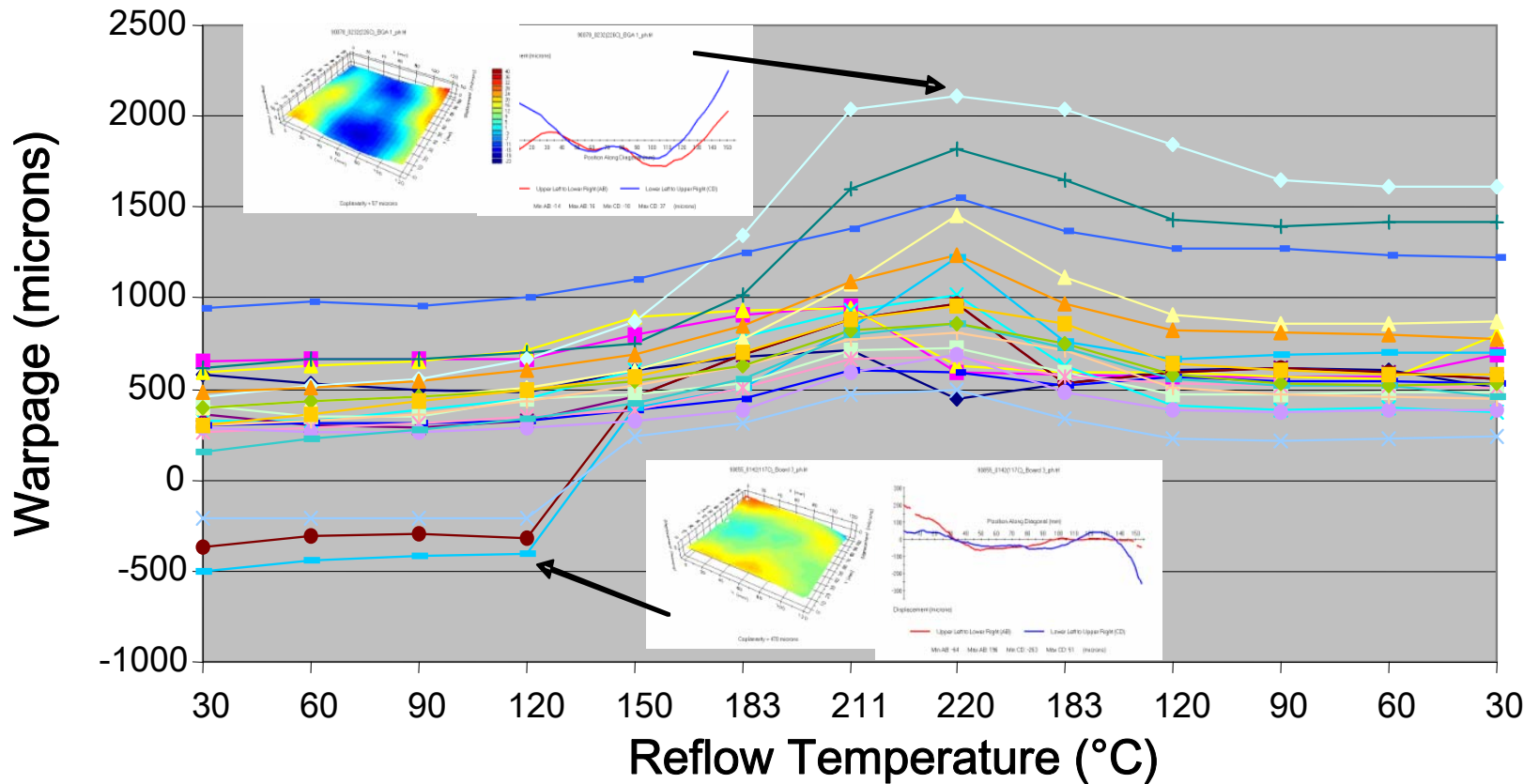


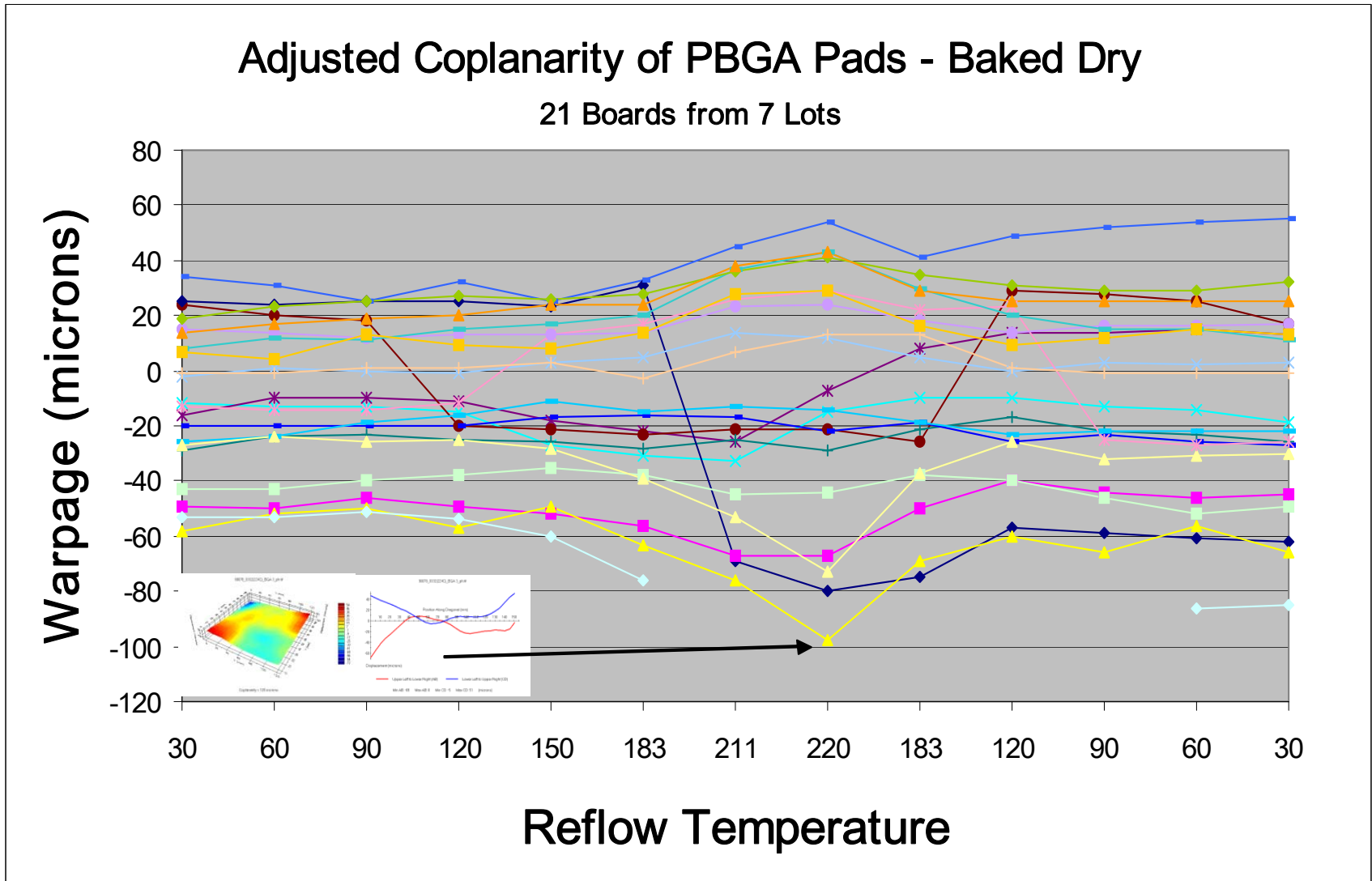
Adjusted Warpage of PBGA Pad Area During Reflow Sampled Directly from Production - 24 Bds from 8 Lots



Circuit Board Warpage - Baked Dry

21 Bds from 7 Lots

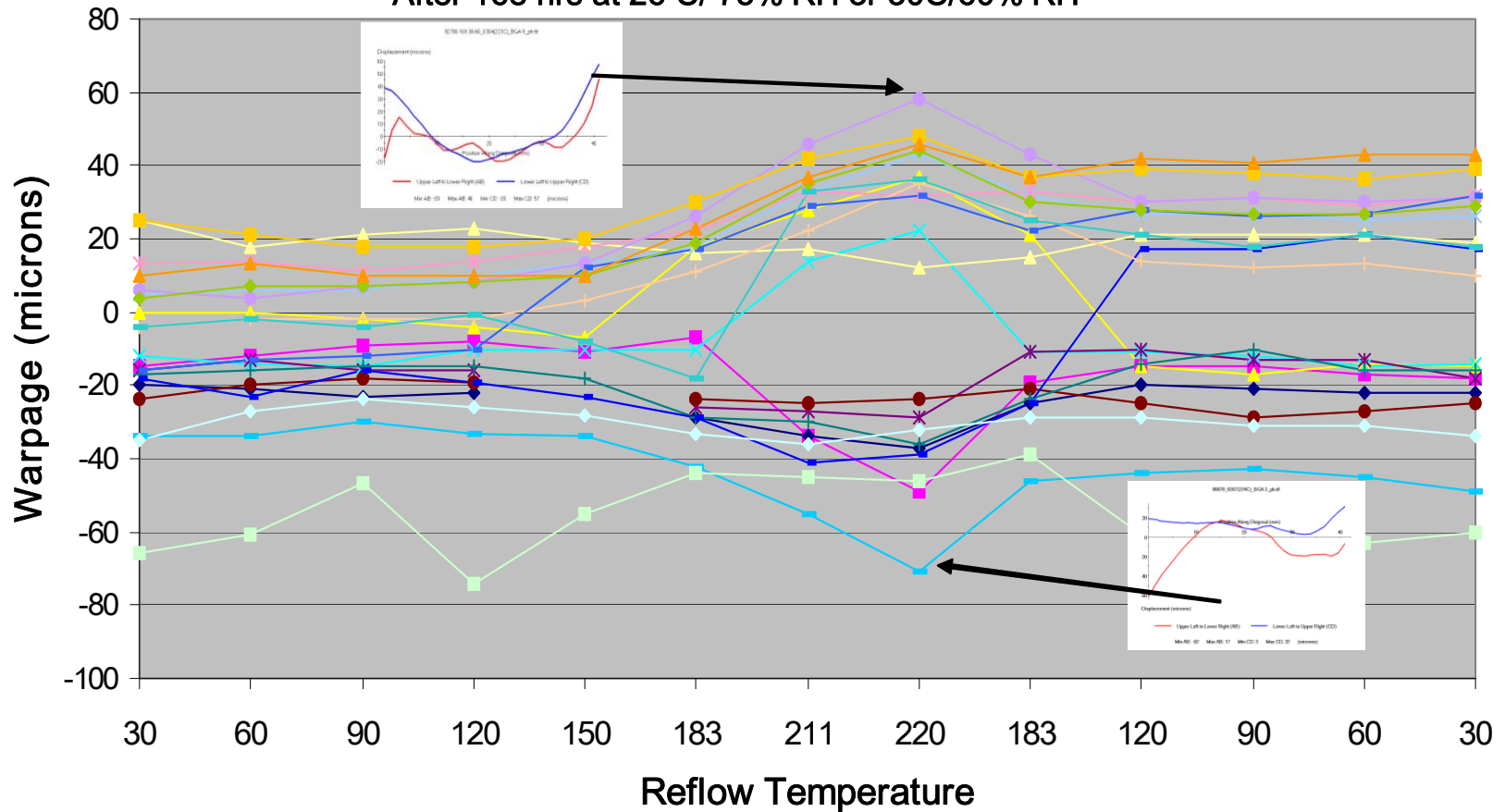




After 168 hrs at 26C /75% RH or 30C/60% RH

Adjusted Warpage of PBGA Area of Board

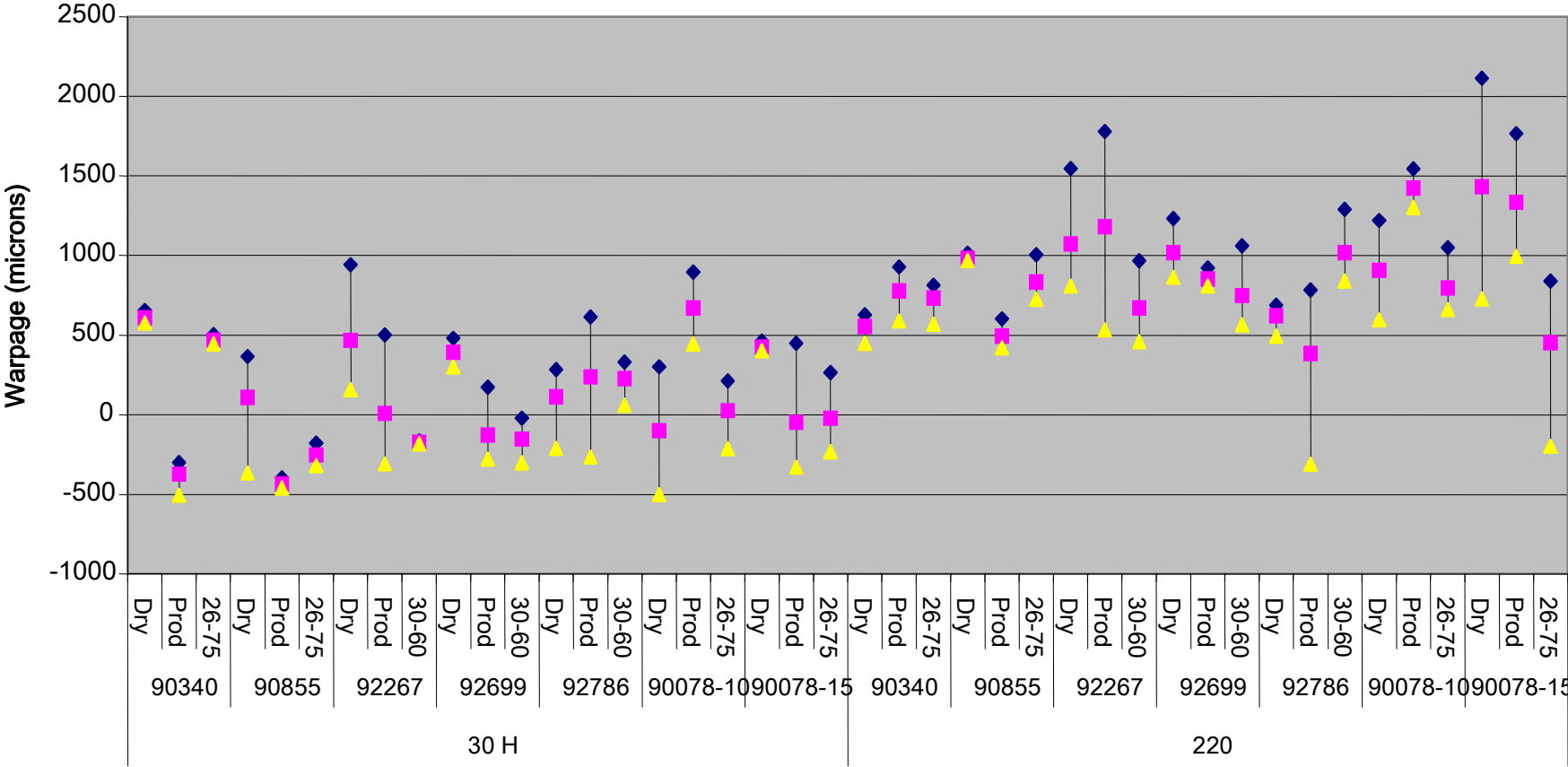
After 168 hrs at 26 C/ 75% RH or 30C/60% RH



Multi-Variate Summary of Board Warpage

Warpage of Circuit Board versus Moisture Conditioning

3 Samples per Condition

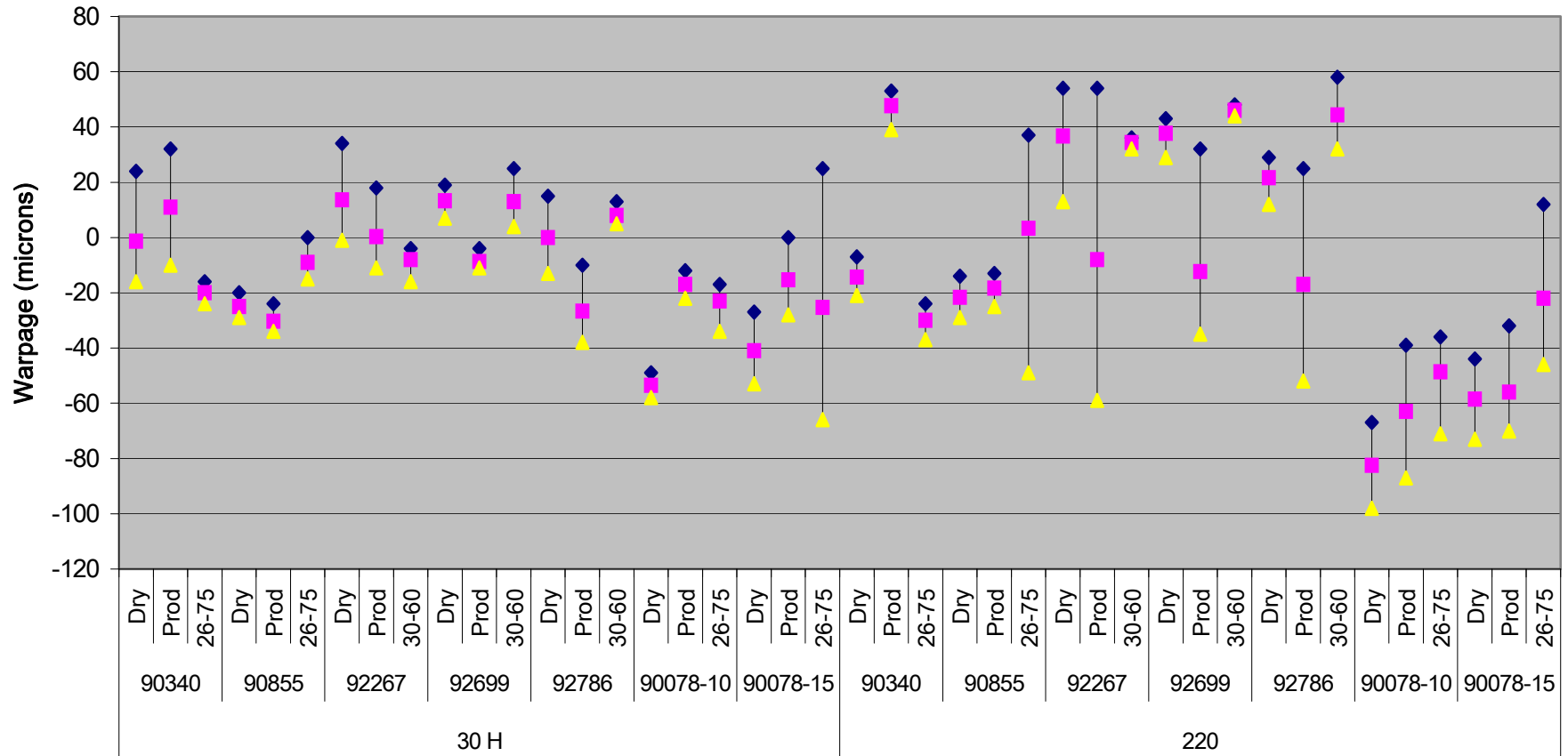


Data		
◆ Max of Warpage	■ Average of Warpage	▲ Min of Warpage

Multi-Variate Summary of PBGA Area Warpage

PBGA Area of Board vs Moisture Conditioning

3 Samples each Condition

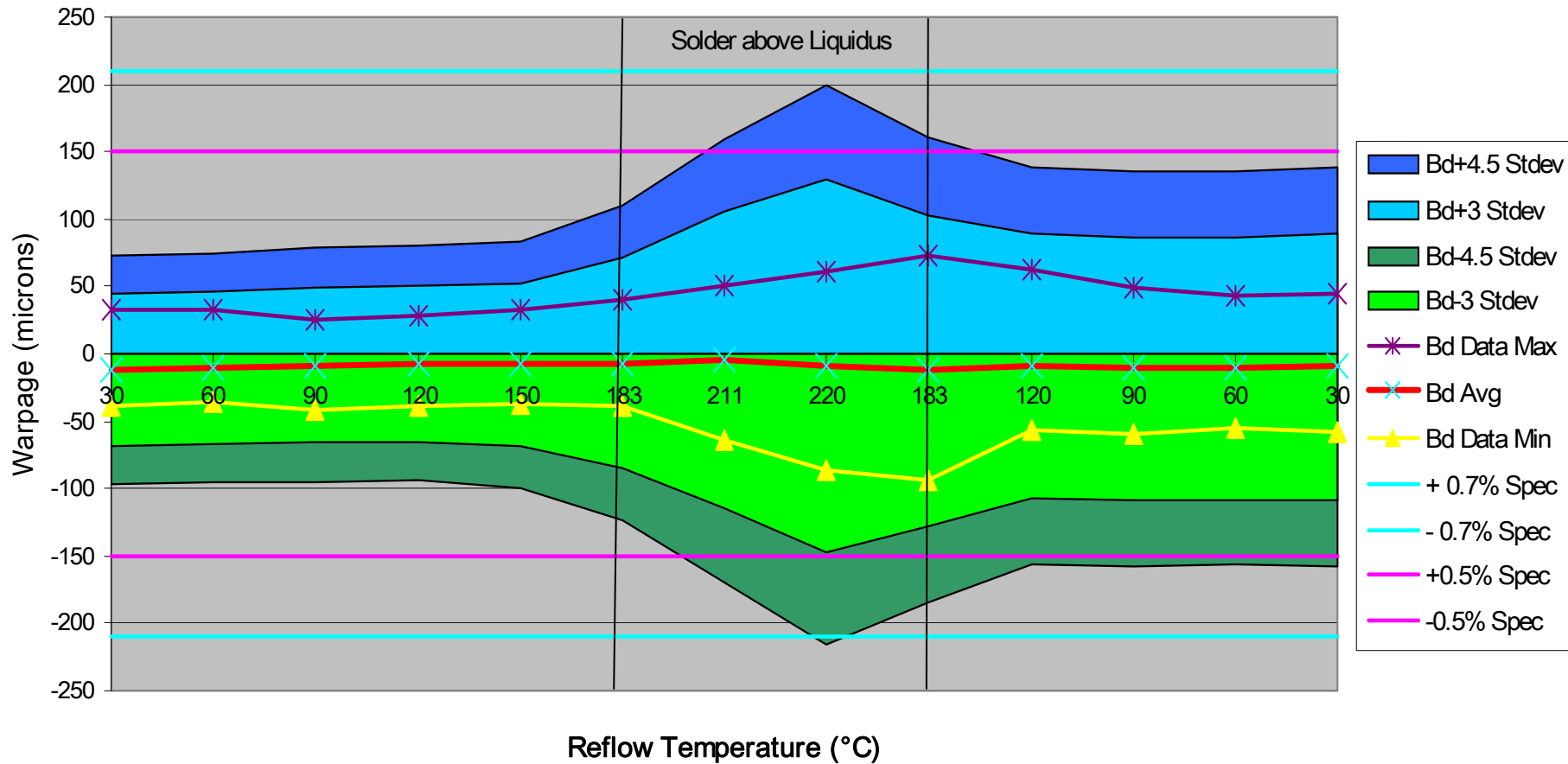


Data

◆ Max of Warpage ■ Average of Warpage ▲ Min of Warpage

Temperature Lot Condition

Statistical Prediction of 30 mm sq PBGA Area Board Warpage - SnPb Reflow Profile



- ◆ Warpage Varies Significantly by
 - Lot
 - Board
 - Moisture Content
 - Reflow Pass (Starting in Production Condition)
- ◆ Effect of Moisture Content Is Not Consistent
 - Effect is Significant within a Lot
 - Optimal Condition Varies by Lot, but generally baked dry is worse
- ◆ Warpage of PBGA Area is Large Enough to Impact PBGA Assembly Yields of Large BGAs
- ◆ Pb-Free Reflow profiles will cause more warpage
- ◆ This study was only single part number / single supplier

- ◆ Develop Standardized Characterization Methodology
 - Sampling Methodology
 - » Random versus Panel / Position
 - » # Lots
 - » # Samples per Lot
 - Moisture Conditioning? Conditions
 - Characterization Temperatures
- ◆ Characterize Additional Part Numbers
- ◆ Characterize Pb-Free Reflow Profile
- ◆ Determine Acceptable Warpage Specifications
 - Solder Reflow Assembly Process Capability
 - » SnPb
 - » SAC
 - Allocate Total Warpage Allowance Between Board and BGA
 - » Optimize Board Cost / Supply / Industry Standards
 - » BGA Cost / Supply / Industry Standards