CSP BOARD LEVEL RELIABILITY - RESULTS

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ABSTRACT
The fatigue and damage of solder joints of area array components as well as the potential for interface failure within chip scale packages (CSP with flex, rigid respectively ceramic interposer) are primarily caused by thermal loading (ambient and/or operating conditions). The thermally induced residual stresses depend on the CTE- mismatch encountered during thermal cycle tests (TCT) and, for power cycle tests (PCT), also on the gradient of the temperature distribution. In order to characterize the potential for failure TCTs and PCTs were used to analyze the board level reliability of different area array components. The reliability is the result of the interaction of different materials and interfaces on component side as well as on board side. For BGAs a lot of fatigue tests are described up to now. Selection guides based on package size, die size, laminate, thickness of interposer, mold thickness, numbers of ball rows, array type etc. are published. The paper outlines CSP package analysis in comparison to BGA types of area array packages. The important point of interest is the applied interposer, the influence of package level interfaces, geometry, package constitution, ball array on the board level reliability. On test- and functional boards the electrical continuity was studied under different test conditions. The successful and safe development of increasingly miniaturized microelectronic structures, such as CSP packages, requires a twofold validation process based on package level and board level qualification. Only the combination of both allows to quickly react to the rapid development of new structures and to actively define the process of their future evolution. Within the pre-reflow "package qualification" the warpage analysis is used to describe the strain and stress level in the package and in the occupied pad area on board. With combination of warpage measurements after reflow simulation and detection of the z-displacement of the package after solder solidification, results regarding the permanent deformations are available describing mechanical strain/stress in the package, ball solder joints and board.

The z-displacement level (strain / stress) is one of the inputs for interpreting on- or offline detected electrical discontinuities. For this reason specially wired boards were used for extended test trials. Studying the board level reliability different board types (conventional, high density laminates; different core materials and µvia-technologies) were used analyzing the assembly quality and the reliability. The kind of board used to assemble CSP on board is a concern. Weibull-plots offer the possibility to compare reliability and lifetime data on BGA side with CSP, depend on board solutions, interconnection quality and aging conditions.

Tests done analyzed various CSP geometry's and materials (flex, rigid and ceramic based interposer). The data for the warpage characteristic of packages, laminates and assemblies as well as the cumulated failure distribution depend on cycles (TCT, PCT) and results of microsections in failed areas/interconnections were used as a basis to generate specific Weibull-plots.

INTRODUCTION
The paper outlines:
- CSP Package analysis in comparison to BGA types of area array packages;
- Influence of interfaces, geometry, package constitution, ball array, interposer, etc.;
- Characterization of laminates used for advanced packages (conventional and HDI-substrates);
- Dimensional stability of substrates depend on constitution, thickness, wiring, adhesion properties, physical data, etc.;
- Characterization of strains and stresses in CSP ball solder joints depend on package type and temperature profiling of the reflow process;
- Warpage analysis depend on package type and substrates, thermal loading of single CSP, occupied areas on board, reflow simulation;
- Interconnection quality depend on package constitution;
- Destructive evaluation examples;
- Warpage behavior of different CSP packages measured on package side and after reflow process; Ranking discussion depend on package type;
- Overview about test files, test strategy, readouts, criteria, interrupts and localization of interrupts, influence of substrates;
- Test files used for reliability studies
- Methods to characterize the degradation behavior of CSP ball solder joints with exploitation of relevant features concerning the reliability;
- TherMoire®, Rodenstock, contact method z-displacement measurement , microsections;
- Microsections of interfaces (first and second level);
- Typical examples characterizing interrupts and/or discontinuities;
- Nondestructive and destructive measurements to describe limitations of the functional stability on board level – exploitation of detected failures Measurements related to electrical test procedures;

- Weibull plots (comparison to conventional devices)

CSP packages tested were based on (leadframe), flex, rigid and ceramic interposer. The main deviation from direct chip attach is the addition of interposer between the silicon and the next interconnection area to which attachment is made. This interposer serve as compliant, space transformer and mechanical protection. BGAs with BT interposer were used to compare lifetime results CSP vs. BGA after TCT and PCT. Table 1 includes an overview about published CSP-tests and results.

From Table 1, it is obvious that each semiconductor supplier has its own test files and conditions depending on application. To compare different packages it seems to be necessary to know more details concerning the board level reliability.

Package	tested by	Test	Testcondition	No. of Cycles / Hours	Failures	Literature
SON26 (Flash ROM)	Fujitsu	TCT (brd.)	-65°C/150°C 24cpd	>500C	0/40	CHR97, Chu97
		TCT (pkg.)	-65°C/150°C 24cpd	500C	0/25	
MCSP96	Mitsubishi	TCT(brd.)	-40°C/125°C, 1h	500C	0/20	CHR97
MCSP96 /w Underfiller		TCT(brd.)			0/3	
CSP40 (DRAM)	Hitachi	TCT(brd.)	-55°C/125°C	1500C	0/21	CHR97, Chu97
µBGA46 (4Mb FLASH)	Intel Co.	TCT(Ceramic brd.)	-65°C/150°C	1000C	4/78	Gre96, RI97, Chu97
		TCT(FR4 brd.)	-55°C/125°C	1000C	0/78	
BLP28 I (16Mb DRAM)	LG Semicon	TCT(brd.)	-55°C/125°C (MIL883C Cond.B)	1000C	11/11	YGKS+97
BLP28 II (16Mb DRAM)		TCT(brd. Padvar.1)			5/6	
		TCT(brd. Padvar.2)			6/6	
		TCT(brd. Padvar.3)			4/6	
CSP48	Sharp Corp.	TCT(brd.)	-40°C/125°C	900C	0/20	KY+97
CSP160				500C	1/5	
CSP180				500C	0/22	
µBGA172	Shinko Corp.	TCT(brd. Padvar.1)	-55°C/125°C 5'/5'	1500C	0/6	Abe96
			-65°C/150°C 30'/30'	1500C	0/6	

Table 1 Accelerated Lifetime Test – Published CSP Board Level Reliability Test Data

CSP Packages (geometry, package constitution, ball array, interposer)
To analyze package constitution driven degradation features the CSP packages listed in Table 2 were used in the lifetime test. The important parameters CSP dimension, interposer & thickness, die dimension, die thickness, first level characterization are presented. The objectives in this paper are as follows: First, it is intended to electrically analyze the board level reliability as well as the first level behavior of differently structured but fully assembled CSP-packages when subjected to thermal cycling between high and low temperature levels (-20°C to +100°C; -40°C to +125°C) as well as to power cycle tests. Quantities of interest include thermal stresses and strains which develop in the various layers of the structures, a quantitative assessment of the influence of defects responsible for electrical discontinuities or interrupts, such as debonding or imperfections in the glue, accumulation of irreversible plastic and creep strains in the solder balls, as well as identification of particularly heavily strained regions within the solder. These results will be tested with real structures on board level.

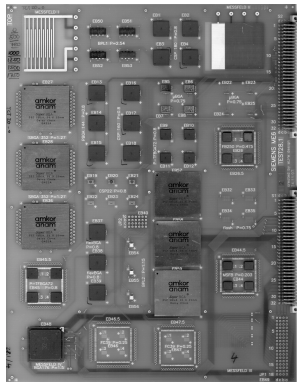
Package	TB	Interposer (Material & Thick. µm)	Dimensions					1.Level	Daisy Chain (DC)
			Pitch (mm)	No. of I/O	Package L x B (mm x mm)	Chip L x B (mm x mm)	Chip Thickn. (µm)		
CSP-f-1	A	PI 50	0,8	180	12x12	10,4x10,4	300	Au-WB	yes
CSP-f-2	A	PI 50	0,8	72	8x8	6,24x6,24	300	Au-WB	yes
CSP-r-1	A	C 400	0,8	160	13x13	9,34x9,55	300	Au-WB	no
CSP-r-2	A	C 400	0,8	22	5x3,8	1,55x1,55	280	C4	no
CSP-r-3	A	BT 200	0,8	161	13x13	9,34x9,55	300	Au-WB	no
CSP-f-3	A	PI 75	0,75	46	5,7x7,8	5,25x7,4	430	CuAu-lead	yes
BGA-r-1	A	BT 970	1,27	352	35x35	13,23x13,23	330	Au-WB	yes + R
FC-1	A	-	0,475	48	-	6,3x6,3	575	-	yes
FC-2	A	-	0,203	96	-	5,6x6,4	575	-	yes
CSP-f-3	B	PI 75	0,8	160	12x12	10,4x10,4	300	Au-WB	yes
CSP-f-4	B	PI 75	0,8	160	12x12	10,4x10,4	300	Au-WB	yes
CSP-f-5	B	PI 50	0,8	72	8x8	6,5x6,24	300	Au-WB	yes
CSP-f-6	B	PI 50	0,8	72	8x8	6,5x6,24	300	Au-WB	yes
CSP-f-7	B	PI 50	0,8	160	12x12	9,6x9,1	285	Au-WB	no
CSP-fr-1	C	PICU 80	0,5	216	15x15	8x7,6	375	TAB	yes
CSP-f-8	C	PI 50	0,75	48	8,03x10,42	6,53x8,92	280	CuAu-lead	yes
CSP-f-1	C	PI 50	0,8	180	12x12	10,4x10,4	300	Au-WB	yes
CSP-r-3	C	BT 200	0,8	161	13x13	9,34x9,55	300	Au-WB	no
CSP-f-9	C	PI 37	0,8	48	5,7x7,8	5,25x7,4	430	CuAu-lead	yes
CSP-r-4	D	C 400	0,8	144	11x11	6,7x6,7	300	Au-WB	yes
CSP-r-3	E	BT 275	0,8	160	13,04x13,04	5,3x5,2	280	Au-WB	funct.
CSP-f-3	E	PI 75	0,8	160	12,15x12,15	7,31x6,87	320	Au-WB	funct.
Package: f-flexible, r-rigid, Interposer: PI-Polyimid, BT-Bismaleimide triazine, C-HTC Ceramic; 1.Level: WB-Wire Bond									

Table 2: Overview-CSP Package Data – Board Level Reliability

Three different CSP packages were considered which differ in the type of substrate that was used and the number of rows of balls along the perimeter: (a) PI-flex, (b) ceramic, and (c) an BT-resin laminate. Details of the dimensions were specified by the manufacturers and, in addition, micro-graphs of the cross-sections were used to obtain accurate geometry data, in particular for the solder balls after reflow. All CSP tested were microsectioned before testing to know the package constitution and the interfaces responsible for stress accumulation. Details describing the CSP are listed in Table 2.

Testboards and Test-Conditions for Board Level Reliability Tests
Table 3 shows one of the applied test boards and gives details about materials (conventional, HDI), finishes, NSMD-pads and additional parameters.

The usual CSP outer ball pitch is not less than 0,5 mm (see Table 2), which avoids some of the board assembly problems. However, problems arise because CSPs are usually assembled jointly with conventional packages. The thermal mass differences between CSP and conventional packages must be taken into account.



general data for all boards	
No. of Layer	4
Solder mask	NSMD
Surface finish	Cu-NiAu
Placement	single-sided
	Material
Board A,B,C,F	FR4
Board D	FR5
Board F	HTG-FR4
	Testboard
board w. stiffener	C
conv. technology	all
SBU technology	C,E,F

Table 3 Data of Testboards

The assembly-related issues (solder volume, laminate pad size and shape, NSMD, ball height) are included in Figure 1 together with remarks related to solder paste wet thickness and reflow profiling.

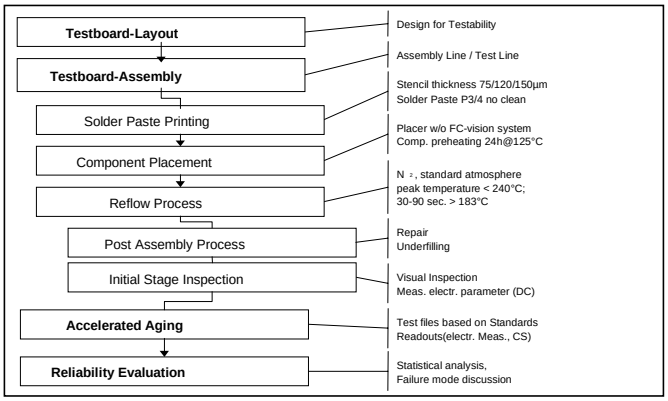


Figure 1 Typical testboard qualification process

Warpage Analysis of CSP Packages

The next part of the board level reliability test, is to detect stresses and strains induced during the various steps of the process flow necessary to produce a CSP structure. The correct choice of material properties and resulting strain and stresses will be measured by TherMoire®-measuring system. This will only characterize surface topography, however, it enables time-reflow temperature profiling. The TherMoire®-characterization is applied on top and bottom side of the CSPs and the thermo-mechanical behavior is obtained. Subjected to tests were CSPs with different dimensions and materials such as interposer to determine z-displacements during the thermal process of interconnecting on board. Figure 2 includes the results in a collected version related to the largest value of z-displacement measured passing the reflow profile. Flex based CSPs are mostly concave warped on top. Rigid interposer based CSPs (top side) offers a warpage behavior as shown in Figure 2 – concave changes to convex warpage at peak temperature depend on T_g of the interposer material. Ceramic based CSPs are mostly convex warped independent from temperature profiling. Therefore different strain and stress levels related to the materials used must be taken into account before analyzing the board level reliability. Figure 2 include the warpage information on the top and bottom side of the CSP.

Warpage comparison of rigid, flex and ceramic CSP-Packages as function of temperatures during reflow process (Diag. center Displacements in µm)

CSP Interposer		flex	rigid	ceramic
CSP:				
Topside	25°C	-41	-13	160
Bottomside		-65	31	-16
(EB Std. FR4)		(21)	(n.a.)	(26)
Topside	220°C	-9	33	148
Bottomside		n.a.(est..: -33)	n.a. (est.: 77)	n.a.(est.: -28)
(EB Std. FR4)		(25)	Delta -44	(n.a.)
		Delta -39		Delta 11
Topside	25°C	-41	-13	160
Bottomside		-72	33	-17
(EB Std. FR4)		(30)	(n.a.)	(27)

Figure 2 Warpage Analysis of CSP (Largest Value of z-Displacement)

Warpage Analysis of Pad Arrays on Board

In the same direction than analyzed CSPs, the pad array on top of the board was measured with the same reflow profile by TherMoire®.

Figure 3 includes the data of z-displacement depend on different laminate qualities (conventional FR 4, HTG-FR 4 and HDI-laminate). The left column describes the actual temperature selected and the following columns the quantity of z-displacement measured. Note the differences in concave and convex warping responsible for non-uniform ball interconnections as well as for strains in interfaces, influencing the delaminations inside the layered board, stresses in vertical electrical interconnections, all responsible for board level reliability.

Warpage comparison of CSP placing areas on Boards of different materials as function of temperatures during reflow process

Board Material	Std. FR4	HTG	HDI (SBU)
Details			Laser-Drilling
25°C	21	-21	-15(-16)
220°C	25	-35	-33(-35)
	Delta : 5	Delta : 16	Delta : 18
25°C	30	-19	-15(-16)

Figure 3 Warpage analysis of laminates used for assembly (largest value of z-displacement)

In the area of interest is the irreversible part of deflection of the board material. The board level reliability of advanced packages depends strictly on the quality of the applied laminate. In the Figure 4 therefore irreversible deformations after

passing the reflow profile were listed by scribing the hysteresis loop for the measured laminate qualities.

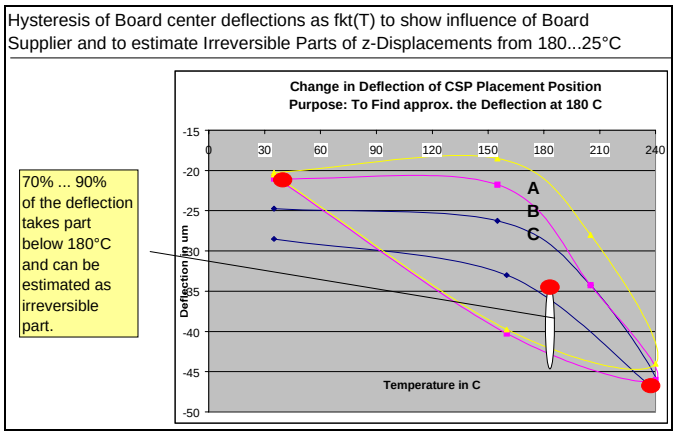


Figure 4 Hysteresis Loop of Displacement Measured on the Top Side (Pad Array) of the Board Material

In Figure 4 the irreversible z-displacement is included after passing the reflow profile. After passing the peak temperature in the cooling period the solidification of the solder used to assemble is responsible for strains and stresses in the board, ball interconnection and in the CSP package. That depends strictly on the laminate (A, B, C) and figures clearly the importance of the right choice of laminates for advanced packages to guarantee customer related reliability features.

Warpage Analysis of Reflowed CSP on Board Level

In addition to the measurements listed above (single CSP, single laminate) the following graph offers the z-displacement measurements of CSP placed in solder paste printed on the pad array on top of the board and soldered related to the reflow profile used in the assembly line (Figure 5). During passing the reflow profile the z-displacement of the top side of the CSP was monitored and related to the board deflection (Figure 3). The left column includes the CSP soldered on conventional FR 4, the following columns the measured z-displacement values for the CSP-top side and the FR 4 pad array. Related to the interposer used in the CSP, different z-displacement results were obtained responsible for non-uniform initial stage characteristics of the reflowed CSP. Between column 2-3 and 3-4 the effective displacements changes are listed which depend on temperature. Furthermore the influence of the solidification temperature of the interconnection solder material limiting the reversible part of deflection (irreversible deformations with impact on stress levels inside the package as well as in the interconnection area). CTE and T_g of mold compound , glue and interposer have direct effects on package performance and reliability. The influence of both is thickness related. Not only the CTE-mismatch and the T_g but also local displacements (delaminations inside the package as well as delaminations in the laminate) are influencing the board level reliability of CSP packages. The stresses may originate with external factors (reflow procedure, changes in ambient and operating temperatures) or internal sources (heat dissipation).

Based on Figure 3 the same simulation for HTG/HDI laminates looks like different and is available for reliability studies.

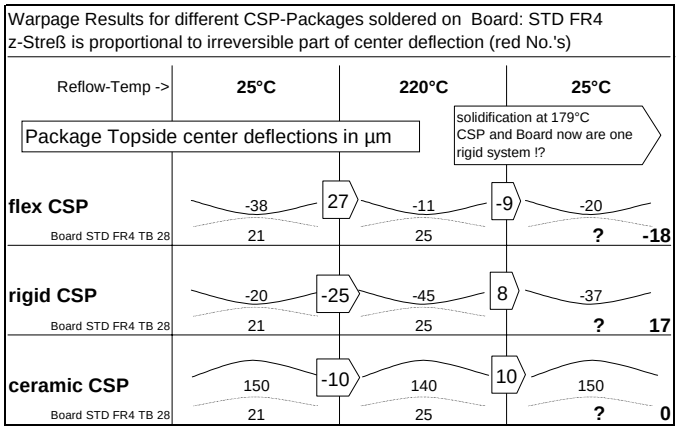


Figure 5 Warpage Analysis of CSP Reflow Soldered on the Board Pad Array (Largest Value of Z-Displacement)

Board Level Reliability - Test Procedures

In Table 4 all the extended trials are listed that were used for the qualification procedure. The incoming tests are also included as well as the test files taken for the board level reliability. Electrical malfunctions or interrupts were consequently analyzed by the tools listed in the Table 4.

Investigations concerning the reliability of advanced packaging and Interconnections			Testboard					
			A	B	C	D	E	F
Analysis (Package & Board Level)	destr./non.	Moisture Absorbtion Measuring	X					
	nondest.	Ball Coplanarity	X					
	destr.	Wetting balance test	X					
	destr.	Reflow test (wettability)	X	X	X			
	nondest.	Warpage meas.(Comp./Board/reflow process)	X	X	X	X	X	X
Failure Analysis after Aging	destr.	Metallography	X	X	X	X	X	X
	destr.	REM(EDX,WDX) on Cross Sections	X	X	X	X	X	X
	nondest.	X-Ray / Laminography	X	X	X	X		
	destr.	Wire Bond peel test	X					
	destr.	Component shear test	X					
	nondest.	Infra red microscopy	X					
	nondest.	Ultra sonic microscopy	X					
Accelerated Lifetime Testing	TCT20	TCT -20°C/100°C 30'10''30'	X	X	X		X	X
	TCT40S	TCT -40°C/125°C 10'10''10'	X			X		
	TCT40	TCT -40°C/125°C 30'10''30'	X	X	X	X	X	X
	TCT40L	TCT -40°C/125°C 60' 3K/min 60'		X	X			
	TCT85L	TCT -40°C/85°C 60' 3K/min 60'		X				
	SN785	TCT SN785	X					
	PCT80	PCT Pv 30'30' @ 80°C	X					
	PCT_rH	PCT Pv 30'30' @ 85°C/85%r.H.		X				
	RH	RH 85°C/85%r.H. @ 1Vbias	X					
	ME	Mechanical shock tests (50g-500g)		X				
	VI	TCT -40°C/125°C 2h 2K/min 2h @ Vibration		X				

Table 4 Test Procedure – Board Level Reliability

The tests taken for accelerated life time studies includes a wide range of test parameters for temperature cycling (different ramp and hold times) and power cycling (different ambient temperatures) and additional tests like 85/85 and mechanical tests.

For all the tests offline-measured electrical data were used to generate Weibull-plots containing important data for the later application.

Electrical Failure Distribution / Weibull-Plots

CSP-components described above were tested under different TCT-conditions. As a precondition to analyze the strain and stress in the first level package note the measurement of the z-displacement (TherMoire®, Figure 2,3,4,5).

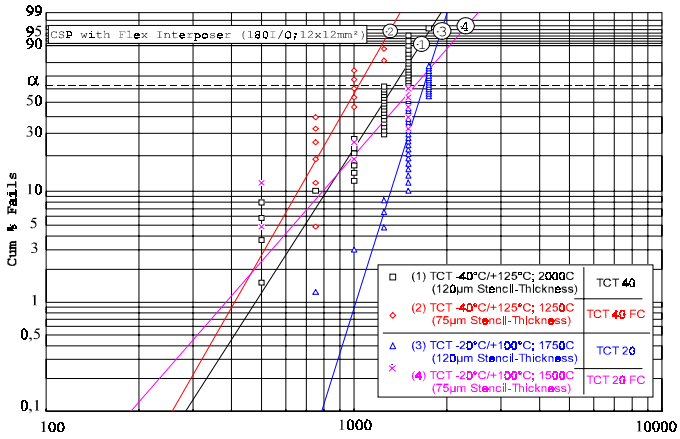


Figure 6 Weibull-Plot Board Level Reliability of flex Interposer Based CSP-f-1 for TCT -20°C/+100°C and -40°C/+125°C (both 30'/10''/30', for Details Table 2, Table 5)

Figure 6 includes data measured for flex CSP for different test parameters. In addition, Table 5 offers the Weibull-parameters calculated on the basis of Figure 6.

CSP-f-1; flex interposer; 180 I/O; 12x12mm² ;Testboard A)				
Test	TCT40	TCT40 FC*	TCT20+**	TCT20 FC*
Failure	45	13	44	9
End of Test	2000	1250	1750	1500
N_f (org.)	1360,68	1037,27	1692,49	1578,13
b (org.)	4,41	4,95	9,00	3,25
N_0	0,00	320,00	0,00	0,00
N_1	480,00	496,52	1015,01	382,87
$N_{0,1}$	284,64	407,96	785,42	188,18
* FC - Board with reduced wet solder paste thickness; ** + all tests included				

Table 5 Weibull-Parameters flex-CSP (s. Figure 6)

In the following Table 6 and Table 7 data for ceramic and rigid interposer based CSP are presented and compared to results of BGA packages in Table 8.

CSP-r-4; ceramic interposer; 144 I/O;11x11mm²;Testboard D)				
Test	TCT40 T1*	TCT40 T2*	TCT40S T2	-
Failure	20	20	15	-
End of Test	1000	1000	1300	-
N_f (org.)	802,59	921,97	1216,24	-
b (org.)	6,35	14,24	13,80	-
N_0	100,00	0,00	760,00	-
N_1	406,82	667,46	938,10	-
$N_{0,1}$	302,90	567,63	871,69	-
* - T1/2 represent different assembly processes				

Table 6 Weibull-Parameters ceramic-CSP

CSP-r-3; rigid interposer; 160 I/O; 13x13mm² ;Testboard E)				
Test	TCT20 B1**	TCT40 B1	TCT20 B2**	TCT40 B2
Failure	4	1	5	33
End of Test	2000	2000	2000	2000
N_f (org.)	*13617,16**	-*	*50261,86**	1634,81
b (org.)	*1,22*	-	*0,65*	1,21
N_0				
N_1	*318,50*	-	*41,46*	36,15
$N_{0,1}$	*48,43*	-	*1,18*	5,34
* number of failure to small for a good calculation				
** B1/2 represent different vendors for the testboard				

Table 7 Weibull-parameters rigid-CSP

Testboard and assembly variations are implemented in the results presented in Table 5, 6, 7 and 8.

Comparison CSP / BGA with rigid (BT) interposer (PBGA225 27x27 mm²; PBGAxxx 25x25 mm²; CSP-r-3 13x13mm²)				
Component	PBGA225	PBGAxxx	CSP-r-3 Testboard E	
Test	TCT20	TCT40	TCT20	TCT40
Failure	8	7	5	33
End of Test	7744	2200	2000	2000
N_f (org.)	6982,99	2306,60	*50261,8**	1629,40
b (org.)	8,76	30,19	*0,65*	1,21
N_0	4100,00			0,00
N_1	4861,84	1980,61	*41,46*	36,04
$N_{0,1}$	4494,14	1834,90	*1,18*	5,33
* number of failure to small for a good calculation				

Table 8 Comparison CSP/BGA with Rigid Interposer

Destructive Evaluation

Results after ΔR-monitoring (electrical failures) are listed in Figure 6 and Table 5 for flex interposer based CSP. Note the influence of solder paste thickness and ΔT-level of chose TCT tests. The obtained crack distribution in ball solder joint interfaces depend on die size is illustrated in Figure 7. The knowledge about crack causing mechanisms depend on the package/board constitution is important to implement advanced packages on board level for different applications.

Figure 8 includes further details for flex CSP on Testboard B (Table 2) related to the die size, die thickness, ball height (stand off) and crack propagation after N = 1000 Cycles – 40/+125.

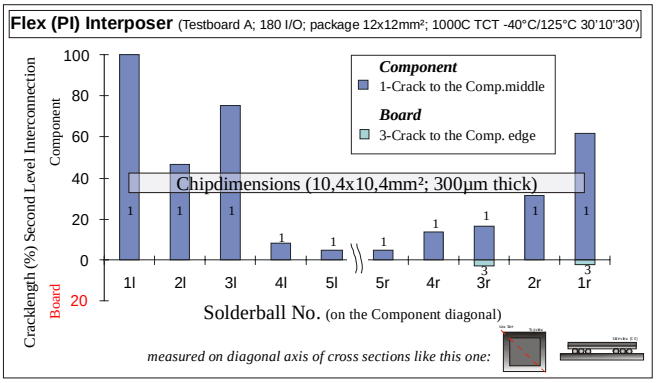


Figure 7 Crack Distribution Analyzed by Destructive Evaluation (Microsectioning) in the Diagonal Axis of flex CSP (CSP-f-1; Testboard A, see Table 2)

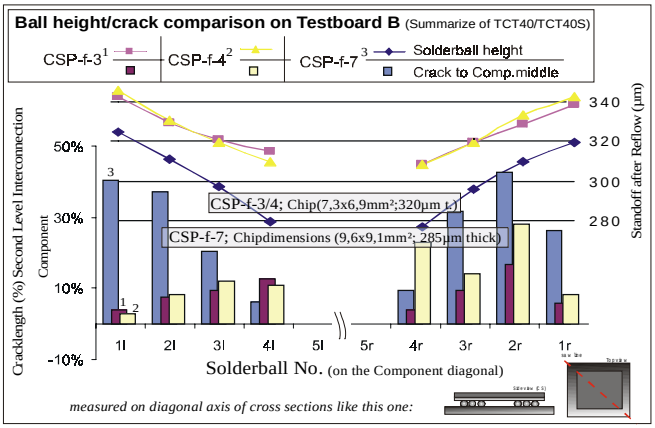


Figure 8 Crack Distribution Comparison Analyzed by Destructive Evaluation (Microsectioning) in the Diagonal Axis of Three Different flex CSP (Testboard B) after TCT –40/+125 N= 1000C

The differences in standoff can be directly related to the warpage measurements before/after passing the reflow oven (Figure 2 and 5).

The crack distribution at the bottom side of the flex CSP (CSP-f-7, Table 2) was analyzed by microsectioning (Figure 9). Once more in relation to the warpage characteristic of the package and the board itself, the standoff after solder solidification is non-uniform, generates non-uniform stress-distribution in the package (delaminations) and the ball array and therefore the risk for electrical discontinuities is not only located in the ball interconnection area, also located in the first level area and in the board used for assembly.

Figure 9 Crack and standoff of ball-interconnections after 1000 Cycle, TCT –40°C/125°C, 30‘10‘‘30‘ (CSP-f-7; Testboard B)

Note the concave warp of the top side of the board as measured in Figure 3. The results presented are taken in the diagonal axis of the soldered component (see schematic view in the graph). In addition to the Weibull-parameter in Table 6 and Table 7 , the crack distribution after destructive evaluation for rigid CSP and ceramic CSP are presented in the following figures.

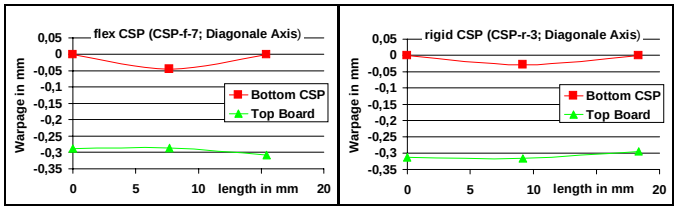


Figure 10 Z-Displacement between Bottom CSP and Top Board, Measured after Microsections; flex CSP (CSP-f-7) Board: FR4; rigid CSP (CSP-r-3) Board: HDI-FR4

Warpage measurements during/after reflow cannot answer the question of board pad array displacement after reflow (right columns, Figure 5), since they refer only on top of the CSP. These information can be taken from microsections like Figure 8. Results for flex CSP (CSP-f-7) and rigid CSP (CSP-r-3) are collected in Figure 10 and allow to analyze the irreversible deformation and the non-uniformity in the soldered ball array.

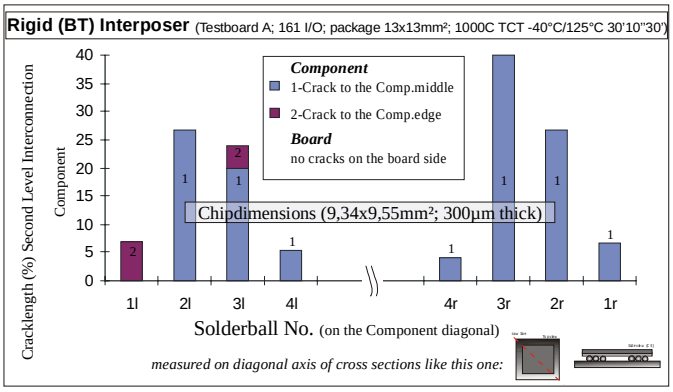


Figure 11 Crack Distribution Analyzed by Destructive Evaluation (Microsectioning) in the Diagonal Axis of laminate CSP (Testboard A)

One ball/ball interconnection after microsectioning at initial stage, after reflow (Table 2) and after TCT -40/+125, N = 2000 cycles, as shown in Figure 12.
Wetting on both sides (top-board and bottom-package) are high enough to fulfill the requirements of stable interconnects. Dendrites (driven by cooling differences in the assembly line) and grain coarsening doesn’t promote degradation significantly. Warpage changing from concave to convex (Package, Figure 2 and reflowed package, Figure 5) obtained for rigid CSP, is limited by solder solidification depended “frozen displacement value”. The ball array connected to the board is more or less much more uniform than detected for flex CSP. On the other hand, flex interposer should be able to compen-

sate strain and stress easier than laminate based interposer. This questions must be answered by taking the Weibull-plots into account. The crack distribution for soldered flex and rigid CSPs is located at the CSP bottom side.

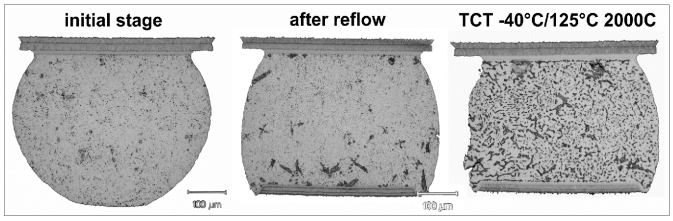


Figure 12 CSP Solder Ball (SnPb63) after Different Aging Steps (Testboard A; CSP-r-3)

Ceramic CSPs are characterized through cracks located at the CSP bottom side (complete interrupts) and laminate top side located cracks (Figure 13). Important for the instability here is the CTE mismatch between package and board. Displacements after passing the assembly line are non-significant. First failure after N = 500 cycles –40/+125 /2/ should be an extended goal for ceramic CSP.

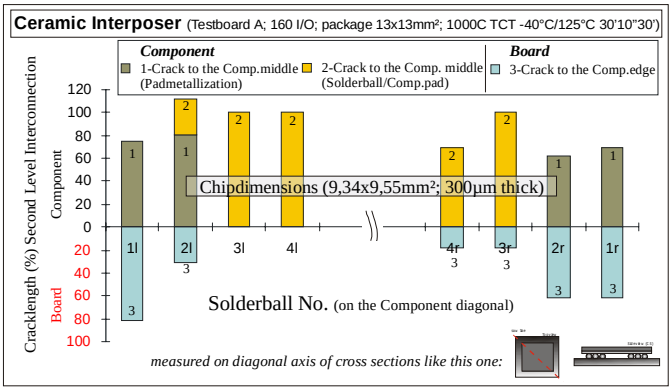


Figure 13 Crack Distribution Analyzed by Destructive Evaluation (Microsectioning); ceramic CSP (Board A)

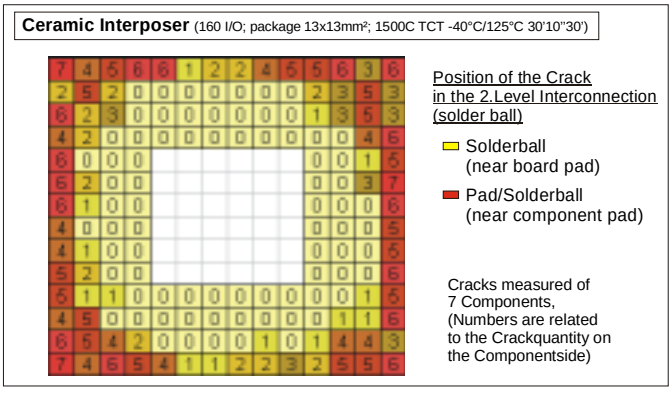


Figure 14 Crack Distribution Over the Whole Ceramic CSP Ball Array (Testboard A)

The distribution of cracks in the interfaces CSP bottom sided ball interconnects and ball interconnects laminate pad side is colored in Figure 14. Clearly marked are the differences to CSP based on flex and rigid interposer.

Lifetime vs. Board Level Reliability

Finally the electrical results will be used to produce a lifetime-reliability ranking chart in which the aforementioned results for CSPs together with data from previous investigations on BGAs will be added. The goal is to obtain a reliability tool from which design rules, geometry factors and choice-of-material recommendations can be deduced.

Consequently, it becomes imperative to check the numerical predictions with results from key experiments performed with the structures in question.

Board level reliability tests on product level are much more important and becomes even more evident if the intent is to quickly assess the fatigue and damage behavior of geometrically highly complex structures, which consist of many different materials, some of which show temperature dependent and highly non-linear material behavior. Moreover, in many cases the material properties and adhesion characteristics are only inaccurately known /3/ or vary significantly when provided by different suppliers. It is very difficult to reliably calculate precisely how many TCT cycles are required to initiate a fatigue crack depend on package constitution. For enhanced flex CSP reliability data were reported with 1000 cycles at –40/+125 at board level /4/. Therefore to predict the lifetime of advanced packages related to "conventional packages" Weibull-plots often used. Table 9 includes reliability data measured for BGA vs. CSP.

CSP (flex / rigid interposer) in comparison to BGA (rigid)
(BGA-r-2 35x35mm²; CSP-f-1 12x12mm², CSP-r-3 13x13mm², CSP-r-4 11x11mm²
Interposer: CSP-f-1 *PI*, CSP-r-3 *BT*, CSP-r-4 *HTCC*, BGA-r-2 *BT*)

Component	CSP-f-1	CSP-r-3	CSP-r-4	BGA-r-2
Test	TCT40	TCT40	TCT40	TCT40
Failure	45	33	20	4
End of Test	2000	2000	1000	2000
N_f (org.)	1360,68	1629,40	921,97	1897,77
b (org.)	4,41	1,21	14,24	5,26
N_0	0,00	0,00	0,00	0,00
N_1	480,00	36,04	667,46	791,18
$N_{0,1}$	284,64	5,33	567,63	510,16

Table 9: Weibull-Parameter Board Level Reliability of flex, rigid and ceramic interposer based CSP vs. BGA for TCT -20°C/+100°C and -40°C/+125°C, 30'/10''/30'

Note the geometrical difference in the "diameter" of solder joints on BGA, CSP and FC for the exploitation too (Figure 15).

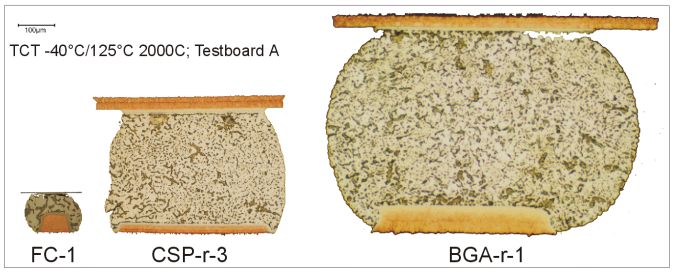


Figure 15 Comparison of Different Solder Ball Sizes

Package sizes must be related to the ball „diameter“ and the ability to compensate strain and stress and a wide range of operating temperature. For FC packages the ball (bump) diameter is decreased significantly and the total amount of grains and/or grain boundaries is decreased too (Figure 16).

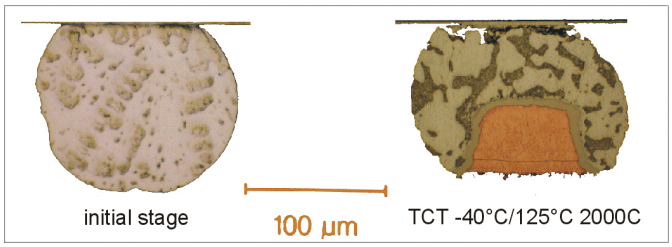


Figure 16 FC Solder Ball (SnPb63) at the Initial Stage and After TCT (Testboard A; FC-1)

Discussion of the Results

- Warpage ranking of CSP with different interposer materials, warpage of occupied areas on board (pad array) and level of irreversible deformations after reflow soldering must be measured for strain and stress characteristics and to select packages for the application needed
- According to the warpage analysis depend on reflow profiling, it exists a connection between interposer used in the CSP package and laminate used to assemble the package. This can be summarized measuring the package and laminate alone as well as after reflow soldering to calculate or measure the irreversible z-displacement after cooling down.
- Various forms of flex and rigid based CSP can accommodate the reliability demands if the package is qualified for extended application temperatures
- For extended temperatures the following Weibull-parameters were calculated and can be used to indentify CSPs needed:
  fCSP, 180 I/O, 12x12 mm^2, pitch 0,8, (N1=480; Nf=1360; β(b)=4,41) – FR 4
  rCSP, 161 I/O, 13x13 mm^2, pitch 0,8, (N1=318; Nf=1631; β(b)=1,21) – HDI
  cCSP, 144 I/O, 11x11 mm^2, pitch 0,8, (N1=406; Nf=802; β(b)=6,35) – FR 5
- Laminates used on board side influencing significantly the board level reliability of CSP (Level of irreversible deformations during/after reflow)
- Global thermal stabilities / instabilities of the whole board (Tg, construction and epoxy/glass/Cu-ratio related) and local CSP related board pad array displacements will influence the ball interconnection area under the uniformity and local strains and is strongly supplier defined.
- Enhanced CSP can fulfill customers need. Increase of first package qualification related to the board level reliability.

CONCLUSIONS

A Change of interposer acts as strategy for decoupling the CTE match between the die and the board level. Interposers like leadframe, flex, rigid and ceramic are common used. Warpage measurements are significant to preferred CSP from the constitution point of view. In addition warpage characteristics of pad arrays on board and during/after reflow soldering the assembly must be taken into account to make the right choice.

Reducing stresses caused by differential expansion in the first and second level is of paramount importance in failure prevention.

Technical evaluation of different CSP types under board level conditions were made to predict the lifetime in comparison to BGA.

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